

Model Name: GA-B85M-D3H

www.xinxunwei.com 400-800-9990

SHEET	TITLE	Revision 1.0
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU_LGA1150-A	
05	CPU_LGA1150-B	
06	CPU_LGA1150-C	
07	DDR III CHANNEL A 1,2	
08	DDR III CHANNEL B 1,2	
09	PCH_FDI,DMI,USB,PCIE,NVRAM	
10	PCH_DP,CLK BUFFER	
11	PCH_HOST,SATA,PCI	
12	PCH_GPIO,CTRL,AUDIO	
13	PCH_PWR,GND	
14	PCI EXPRESS*16 SLOT	
15	PCI EXPRESS*4 SLOT	
16	PCI SLOT1,2	
17	ITE 8728 LPC IO	
18	COM,KB_MS_USB,USB30_20	
19	HWM,FAN CTRL,OV,-PROCHOT	
20	DUAL BIOS	
21	FP,FUSB,SPK,SATALED	
22	Realtek ALC892-GR	
23	REAR AUDIO JACK	
24	REALTEK RTL8111F	
25	DISCRETE POWER	
26	ATX , CLOCK GEN, TPM	
27	VCORE ISL95820_1	

SHEET	TITLE
28	VCORE ISL95820_2
29	RT8120_DDR POWER
30	LPT, M3 POWER
31	DVI, HDMI
32	IT8892E

Gigabyte Technology		
Title		
Cover Sheet		
Size	Document Number	Rev
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Revision 1.0
P-Code U12090-0

[illegible]

BLOCK DIAGRAM

PCI EXPRESS X16

DVI, HDMI

RGB

PCI EXPRESS X4

PCI BRIDGE ITE IT8892

Realtek RTL8111F

USB2.0 PORTS X12

USB3.0 PORTS X4

INTEL LGA1150

VRD12.5

PCH (B85)

Realtek ALC892

AUDIO PORTS : FRONT AUDIO
LIN_ OUT LINE_IN MIC CD_IN
SURROUND CEN/LEF SURR BACK

CHANNEL A
DDRIII DIMM X 2

CHANNEL B
DDRIII DIMM X 2

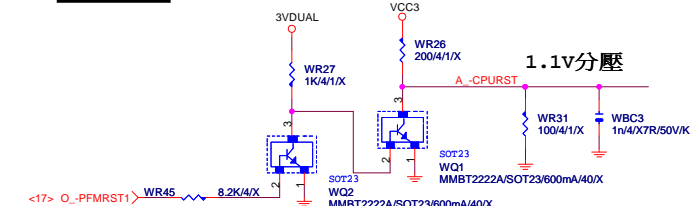
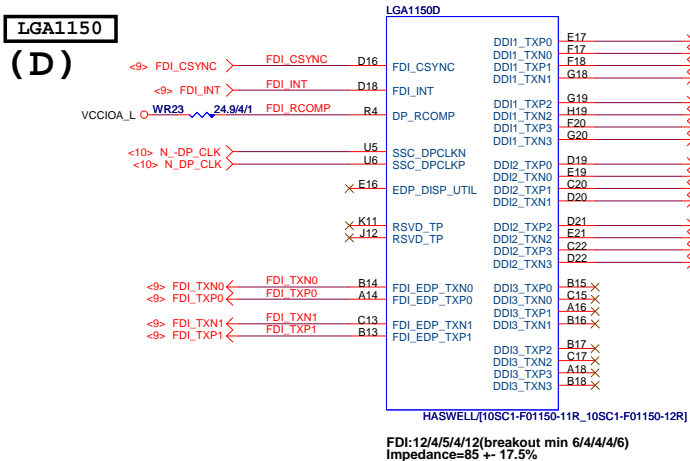
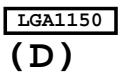
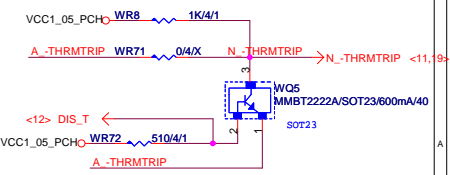
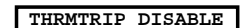
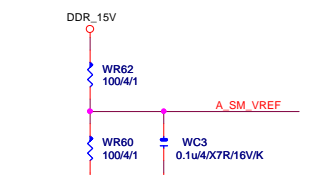
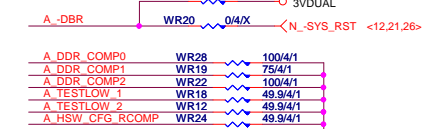
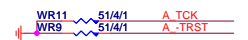
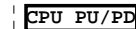
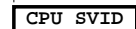
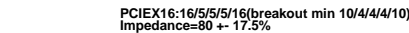
SATAIII*4/SATAII*2

DUAL BIOS

LPC I/O ITE8728

I/O PORTS :
COM KB/MS

FRONT PANEL / FAN

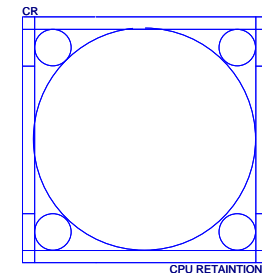


LGA1150A			
MAAA0	AU13	DDRO_D0	AD38 MDA0
MAAA1	AV16	DDRO_D1	AD39 MDA1
MAAA2	AW18	DDRO_D2	AF38 MDA2
MAAA3	AW17	DDRO_D3	AF39 MDA3
MAAA4	AU17	DDRO_D4	AD37 MDA4
MAAA5	AW18	DDRO_D5	AD40 MDA5
MAAA6	AV17	DDRO_D6	AF37 MDA6
MAAA7	AT18	DDRO_D7	AF40 MDA7
MAAA8	AU18	DDRO_D8	AH40 MDA8
MAAA9	AT19	DDRO_D9	AF39 MDA13
MAAA10	AW11	DDRO_D10	AK38 MDA10
MAAA11	AU19	DDRO_D11	AK39 MDA11
MAAA12	AU19	DDRO_D12	AK37 MDA12
MAAA13	AY10	DDRO_D13	AK38 MDA8
MAAA14	AT20	DDRO_D14	AK37 MDA14
MAAA15	AU21	DDRO_D15	AK40 MDA17
		DDRO_D16	AM40 MDA20
MODT_A0	AW10	DDRO_D17	AP39 MDA21
MODT_A1	AY8	DDRO_D18	AM38 MDA18
MODT_A2	AU9	DDRO_D19	AP39 MDA19
MODT_A3	AW8	DDRO_D20	AM39 MDA20
		DDRO_D21	AK38 MDA16
		DDRO_D22	AP37 MDA22
	AW33	DDRO_D23	AP40 MDA23
	AU33	DDRO_D24	AV37 MDA25
	AU31	DDRO_D25	AW37 MDA29
	AU31	DDRO_D26	AK35 MDA26
	AT33	DDRO_D27	AV35 MDA27
	AU33	DDRO_D28	AM37 MDA28
	AT31	DDRO_D29	AT37 MDA24
	AW31	DDRO_D30	AD35 MDA30
		DDRO_D31	AW35 MDA31
<-> SBAA0 <->	SBA0	DDRO_D32	AY6 MDA33
<-> SBA1 <->	SBA1	DDRO_D33	AY6 MDA37
<-> SBA2 <->	SBA2	DDRO_D34	AW4 MDA34
		DDRO_D35	AW4 MDA35
<-> KEA0 <->	KEA0	DDRO_D36	AW6 MDA36
<-> KEA1 <->	KEA1	DDRO_D37	AW4 MDA32
<-> KEA2 <->	KEA2	DDRO_D38	AW4 MDA38
<-> KEA3 <->	KEA3	DDRO_D39	AW4 MDA39
		DDRO_D40	AR1 MDA41
<-> CSA0 <->	CSA0	DDRO_D41	AR1 MDA45
<-> CSA1 <->	CSA1	DDRO_D42	AN2 MDA42
<-> CSA2 <->	CSA2	DDRO_D43	AN4 MDA43
<-> CSA3 <->	CSA3	DDRO_D44	AR2 MDA44
		DDRO_D45	AR2 MDA40
<-> DCLKA0 <->	DCLKA0	DDRO_D46	AN2 MDA46
<-> DCLKA1 <->	DCLKA1	DDRO_D47	AN1 MDA47
<-> DCLKA2 <->	DCLKA2	DDRO_D48	AL1 MDA49
<-> DCLKA3 <->	DCLKA3	DDRO_D49	AL3 MDA53
<-> DCLKA4 <->	DCLKA4	DDRO_D50	AJ3 MDA50
<-> DCLKA5 <->	DCLKA5	DDRO_D51	AJ4 MDA51
<-> DCLKA6 <->	DCLKA6	DDRO_D52	AJ2 MDA52
<-> DCLKA7 <->	DCLKA7	DDRO_D53	AJ2 MDA44
		DDRO_D54	AJ1 MDA55
	AW12	DDRO_D55	AG1 MDA57
		DDRO_D56	AG4 MDA61
		DDRO_D57	AE3 MDA58
		DDRO_D58	AE4 MDA59
		DDRO_D59	AG2 MDA60
		DDRO_D60	AG3 MDA56
		DDRO_D61	AG3 MDA62
<-> -SRASA <->	-SRASA	DDRO_D62	AE1 MDA63
<-> -SWEA <->	-SWEA	DDRO_D63	AE39 DQSA0
		DDRO_D64	AJ39 DQSA1
<-> -SWEA <->	-SWEA	DDRO_D65	AV36 DQSA2
		DDRO_D66	AV36 DQSA3
		DDRO_D67	AV35 DQSA4
<-> -SCASA <->	-SCASA	DDRO_D68	AP3 DQSA5
		DDRO_D69	AP3 DQSA6
		DDRO_D70	AF3 DQSA7
<-> -DDR3_RST <->	WR61 0.1uH/47K/16V/KX	DDRO_D71	AV32 DQSA0
		DDRO_D72	AE38 DQSA1
		DDRO_D73	AN38 DQSA2
		DDRO_D74	AN36 DQSA3
		DDRO_D75	AW5 DQSA4
		DDRO_D76	AP3 DQSA5
		DDRO_D77	AK2 DQSA6
		DDRO_D78	AF2 DQSA7
		DDRO_D79	AF32 DQSA8
		DDRO_D80	AK2 DQSA9
		DDRO_D81	AK2 DQSA10
		DDRO_D82	AK2 DQSA11
		DDRO_D83	AK2 DQSA12
		DDRO_D84	

HASWELL/10SC1-F01150-11R_10SC1-F01150-12R

CGA1150B			
	MAAB0	AL19	DDR1_M0A
	MAAB1	AK23	DDR1_M1A
	MAAB2	AM22	DDR1_M2A
	MAAB3	AM23	DDR1_M3A
	MAAB4	AP23	DDR1_M4A
	MAAB5	AL23	DDR1_D0A
	MAAB6	AY24	DDR1_M5A
	MAA57	AV25	DDR1_M6A
	MAAB8	AU26	DDR1_M7A
	MAAB9	AW25	DDR1_M8A
	MAAB10	AP18	DDR1_M9A
	MAAB11	AY25	DDR1_M10A
	MAAB12	AV26	DDR1_M11A
	MAAB13	AY26	DDR1_M12A
	MAAB14	AV27	DDR1_M13A
	MAAB15	AY28	DDR1_M14A
			DDR1_M15A
	MODT_B0	AM17	DDR1_ODT0
	MODT_B1	AL16	DDR1_ODT1
	MODT_B2	AM16	DDR1_ODT2
	MODT_B3	AK15	DDR1_ODT3
		AM26	DDR1_EC0C
		AM25	DDR1_EC1C
		AP25	DDR1_EC2C
		AP26	DDR1_EC3C
		AL25	DDR1_EC4C
		AR26	DDR1_EC0S
		AR25	DDR1_EC6C
		AR25	DDR1_EC7C
<->	SBA00	SBA00	DDR1_BA0
<->	SBA01	SBA01	DDR1_BA1
<->	SBA02	SBA02	DDR1_BA2
<->			DDR1_BA3
<->	CKE00	CKE00	DDR1_CKE0
<->	CKE01	CKE01	DDR1_CKE1
<->	CKE02	CKE02	DDR1_CKE2
<->	CKE03	CKE03	DDR1_CKE3
<->	CS00	CS00	DDR1_CS_N0
<->	CS01	CS01	DDR1_CS_N1
<->	CS02	CS02	DDR1_CS_N2
<->	CS03	CS03	DDR1_CS_N3
<->	DCLK00	DCLK00	DDR1_CLK_P0
<->	DCLK01	DCLK01	DDR1_CLK_P1
<->	DCLK01	DCLK01	DDR1_CLK_N0
<->	DCLK01	DCLK01	DDR1_CLK_N1
<->	DCLK02	DCLK02	DDR1_CLK_P2
<->	DCLK02	DCLK02	DDR1_CLK_N2
<->	DCLK03	DCLK03	DDR1_CLK_P3
<->	DCLK03	DCLK03	DDR1_CLK_N3
<->	SCASB0	SCASB0	DDR1_CAS*
<->		ALP10	DDR1_RSVD
<->	SRASB0	SRASB0	DDR1_RAS*
<->	SWEB0	SWEB0	DDR1_WE*
<->	VREF_D0A	VREF_D0A	DDR_VREF_D0A
<->	VREF_D0B	VREF_D0B	DDR_VREF_D0B
			DDR1_D0S_P0
			DDR1_D0S_P1
			DDR1_D0S_P2
			DDR1_D0S_P3
			DDR1_D0S_P4
			DDR1_D0S_P5
			DDR1_D0S_P6
			DDR1_D0S_P7
			DDR1_D0S_P8
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			DDR1_D0S_N6
			DDR1_D0S_N7
			DDR1_D0S_N8
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			DDR1_D0S_P2
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			DDR1_D0S_P5
			DDR1_D0S_P6
			DDR1_D0S_P7
			DDR1_D0S_P8
			DDR1_D0S_N0
			DDR1_D0S_N1
			DDR1_D0S_N2

HASWELL/10SC1-F01150-11R_10SC1-F01150-12R



LGA1150_F



ILM_BP/1156/CSP/ILM_BP/1156/CSP/12KRC-0F0001-52R_12KRC-0F0001-51R

DDR BUS

3. MODT_A[0..3] / \ MODT_A[0..3]

MODT_B[0..3]

<7> MDA[0..63] ↔ MDA[0..63]

<8> MDB[0..63] \longleftrightarrow MDB[0..63]

7 DQSA[0..7] ↔ DQSA[0..7]

<7> -DQSA[0..7] ↔ -DQSA[0..7]

MAAAIO 151

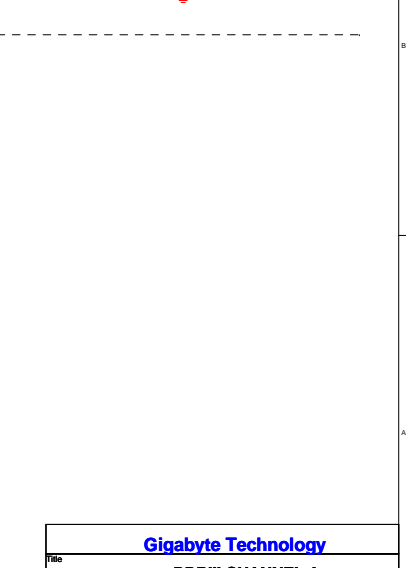
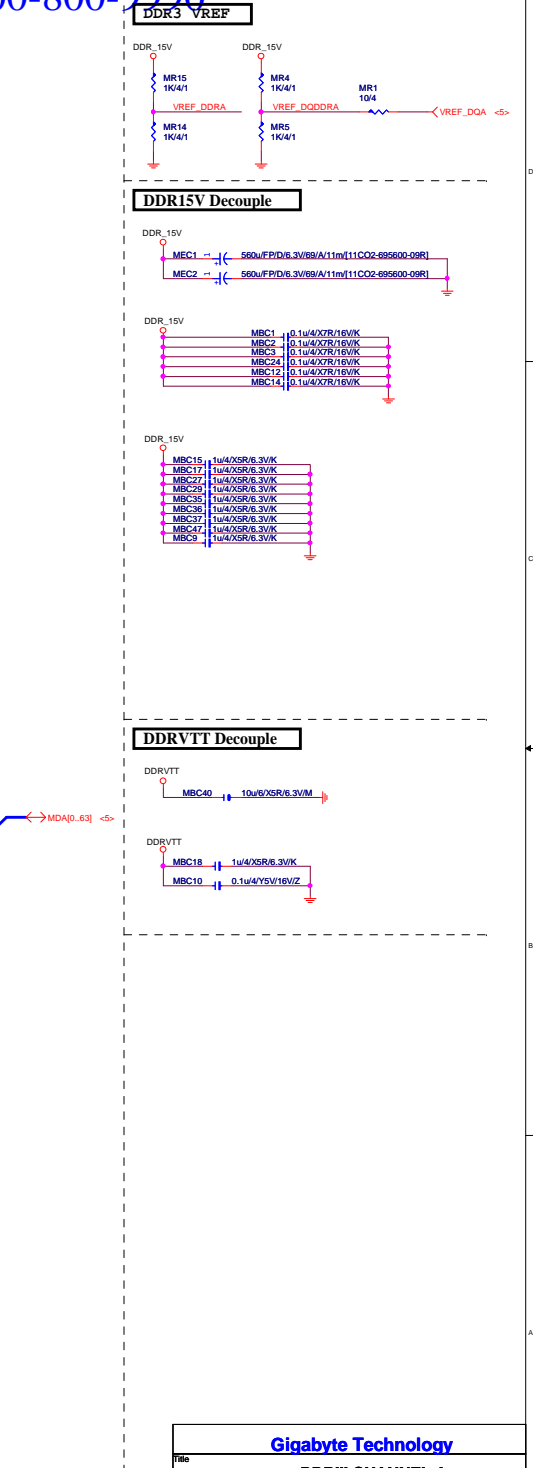
<7> MAAA[0..15] ↔ MAAA[0..15]

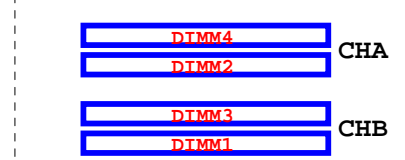
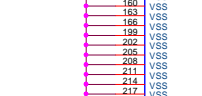
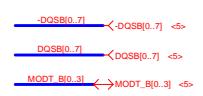
<8> MAAB[0..15] ↔ MAAB[0..15]

----- / \ DQSB[0..7]

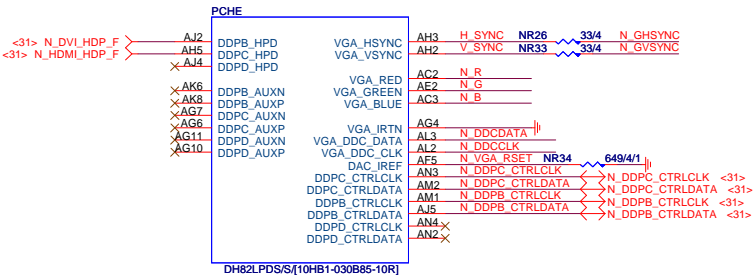
<8> DQSB[0..7] \longleftrightarrow -DQSB[0..7]

<8> -DQSB[0..7] ↔ DQSB[0..7]

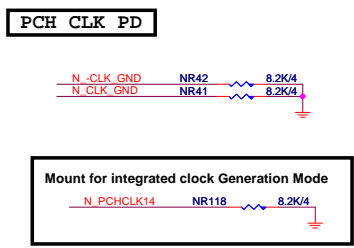
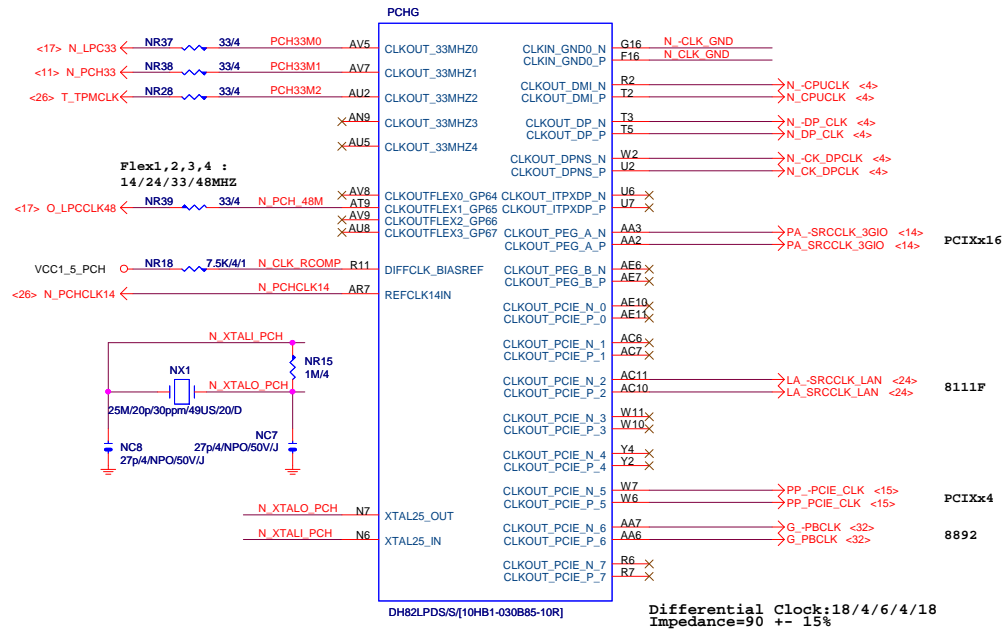




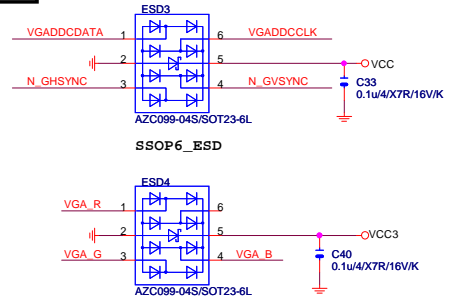
PCH (E)



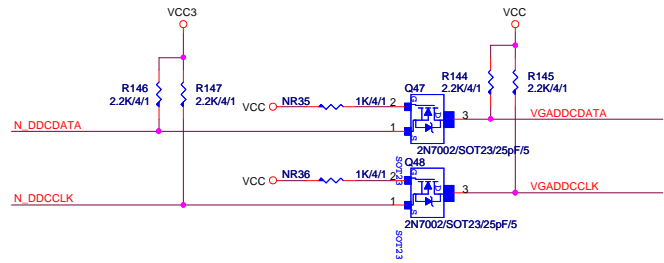
PCH (G)



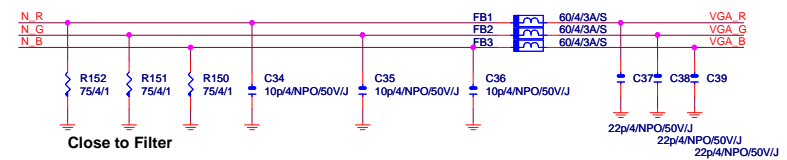
VGA ESD



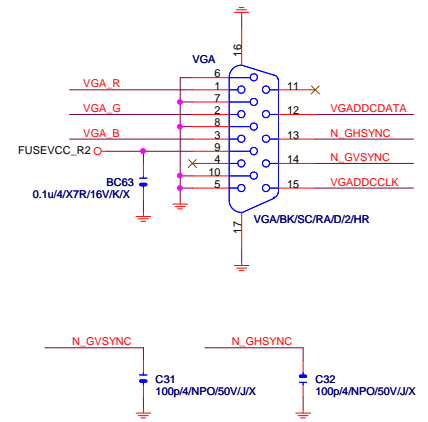
VGA DDC



VGA DDC



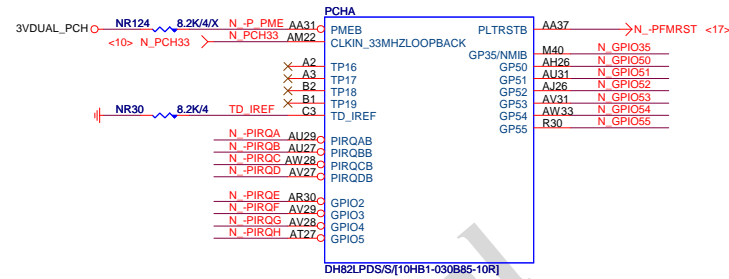
VGA CONNECTOR



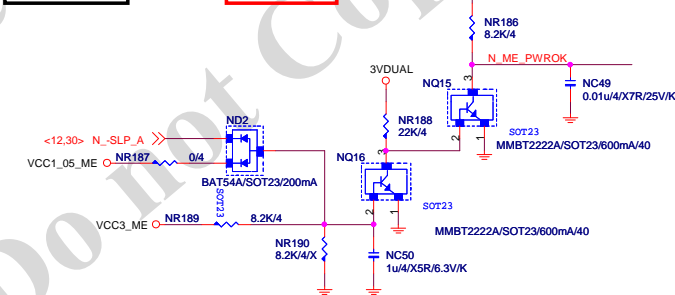
Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
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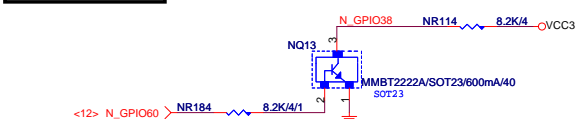
PCH (A)



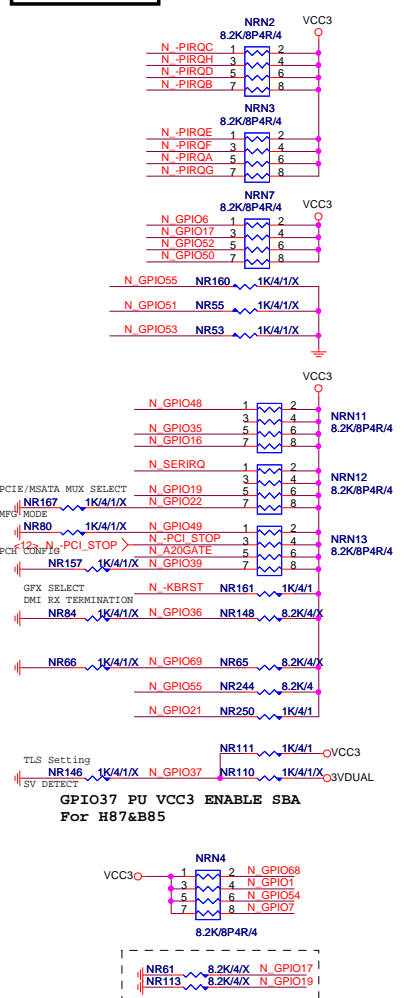
Z87 N/A



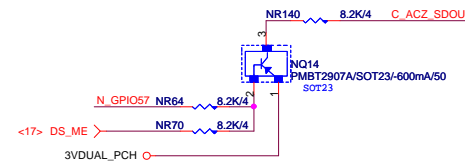
GPIO38 Ctrl



PCH	PU/PD
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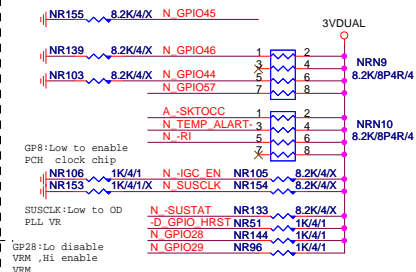
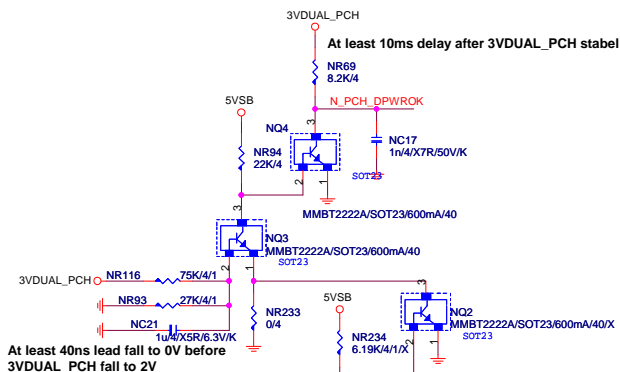


C_ACZ_SDOUT : HI --> ME Enable
Lo --> ME Disable
HI:disable ME and override SOI Flash Access Permissions

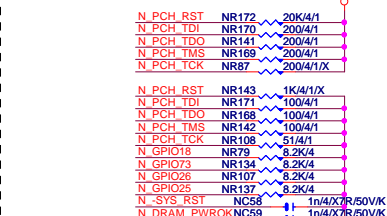
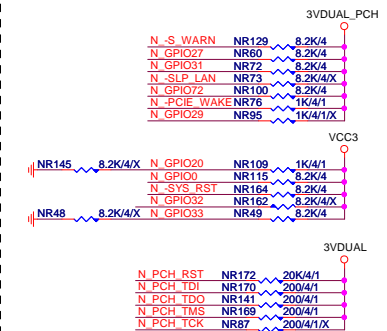


SPI OVERRIDE PROTECTION

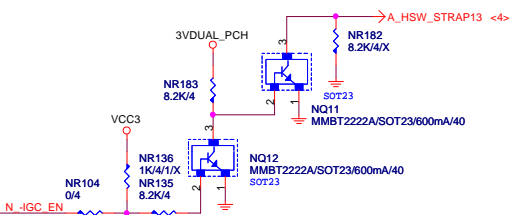
PCH_DPWROK



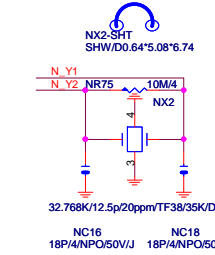
GP28:Lo disable
PLL VR
VPM



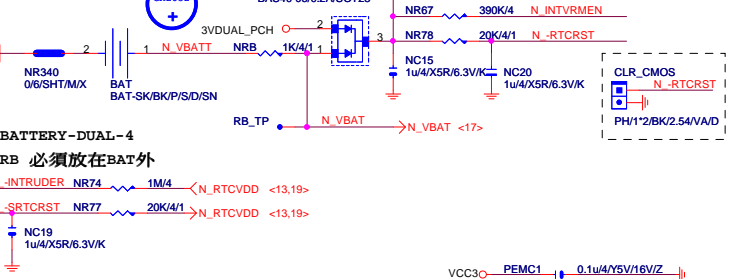
HSW_STAP13



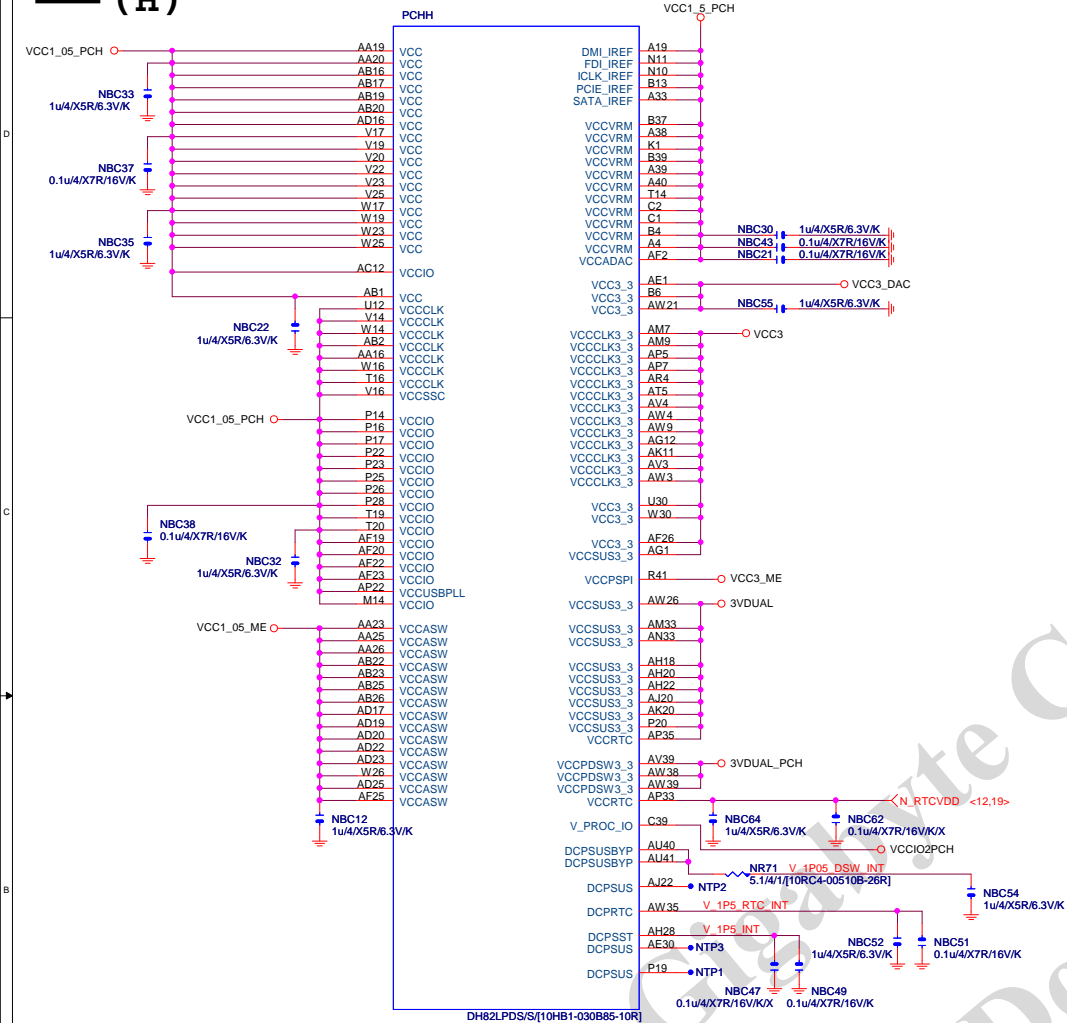
32.768KHZ



CLR_CMOS

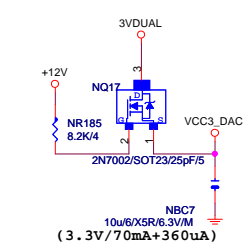


PCH (H)



VCC3_DAC

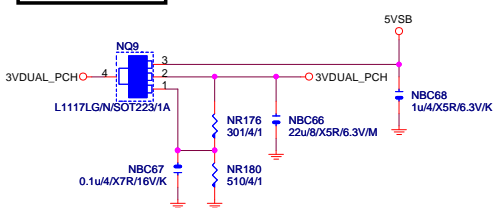
CLOSE北橋(注意震盪水波紋)



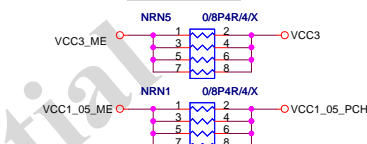
(3.3V/70mA+360uA)



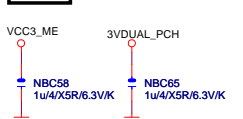
3VDUAL_PCH



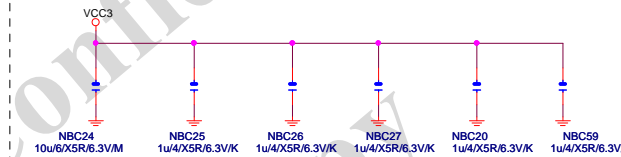
SHT PWR



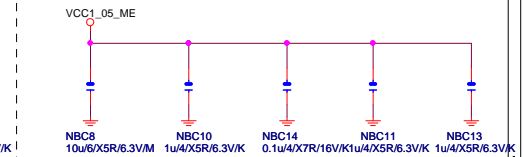
CAP



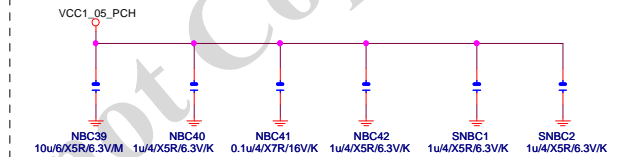
(3.3V) (X6)



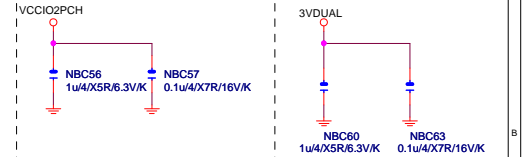
(1.05V) (x5)



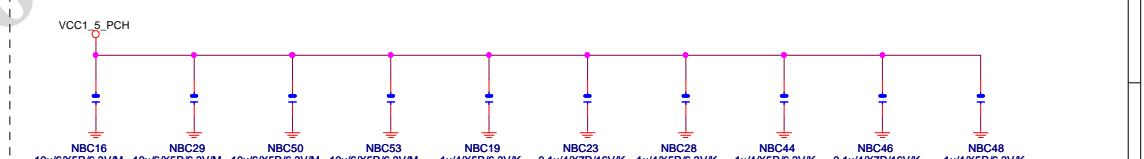
(1.05V) (x6)



(1.05V)(x2) (3.3V) (x2)

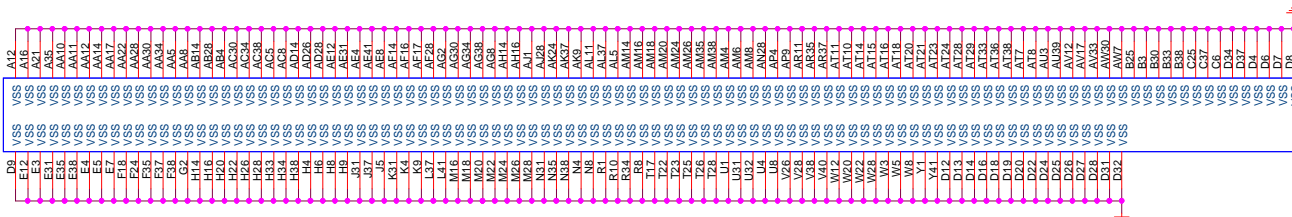


(1.05V) (x10)



PCH

(I)



PCHI
DH82LPDS/S[10HB1-030B85-10R]

Gigabyte Technology

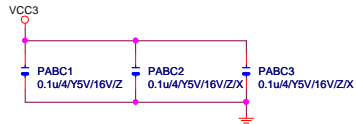
PCH PWR ,GND

GA-B85M-D3H

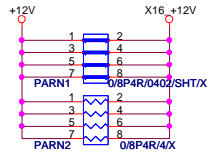
10

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PCIEX16 CAP



PCIEX16 PROTECT SHT

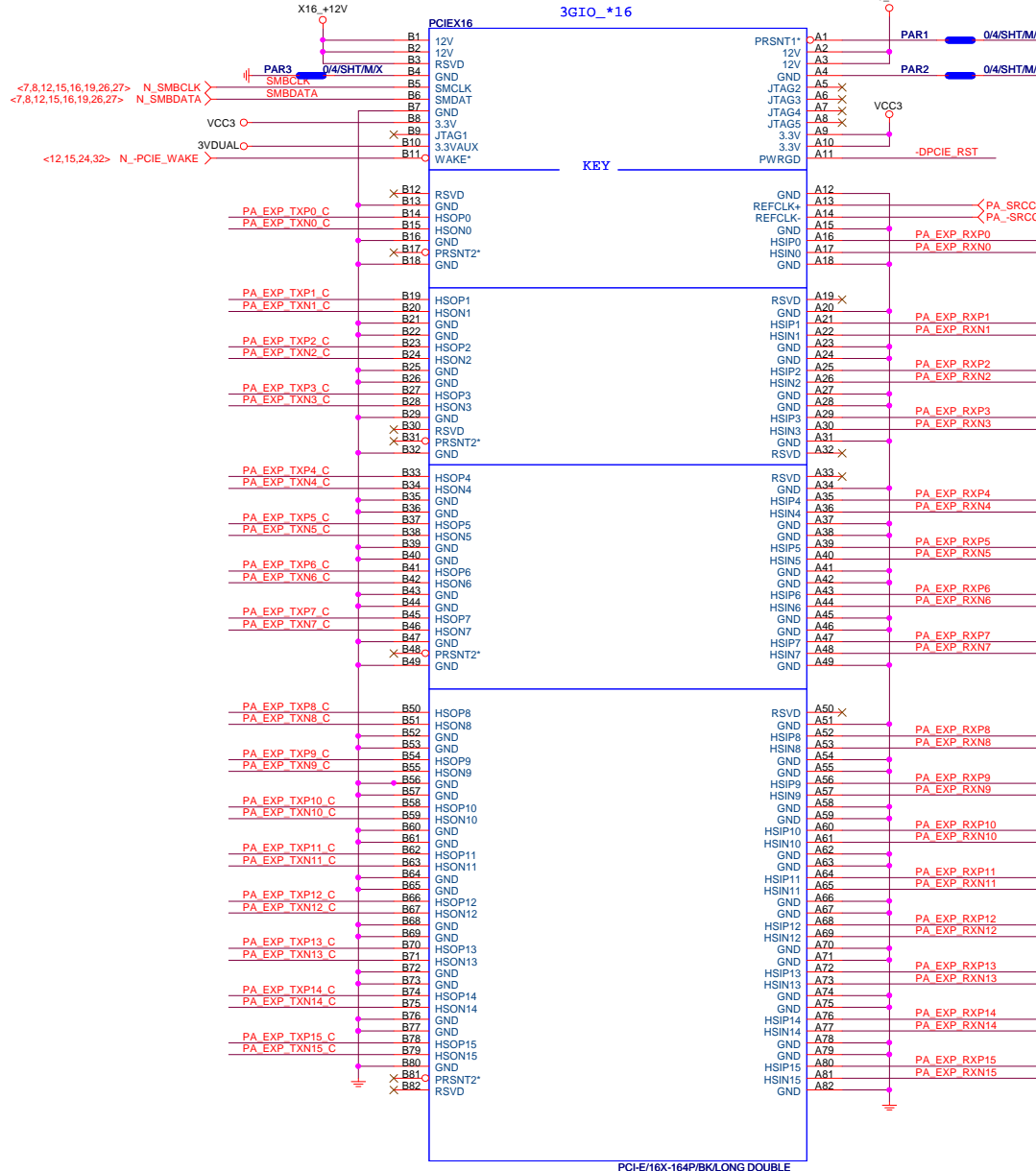


PCIEX16 AC CAP

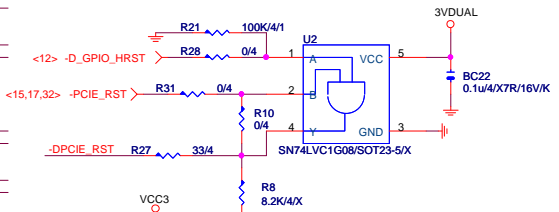
PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] <4>
 PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] <4>
 PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] <4>
 PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] <4>

PCIEX16 SLOT

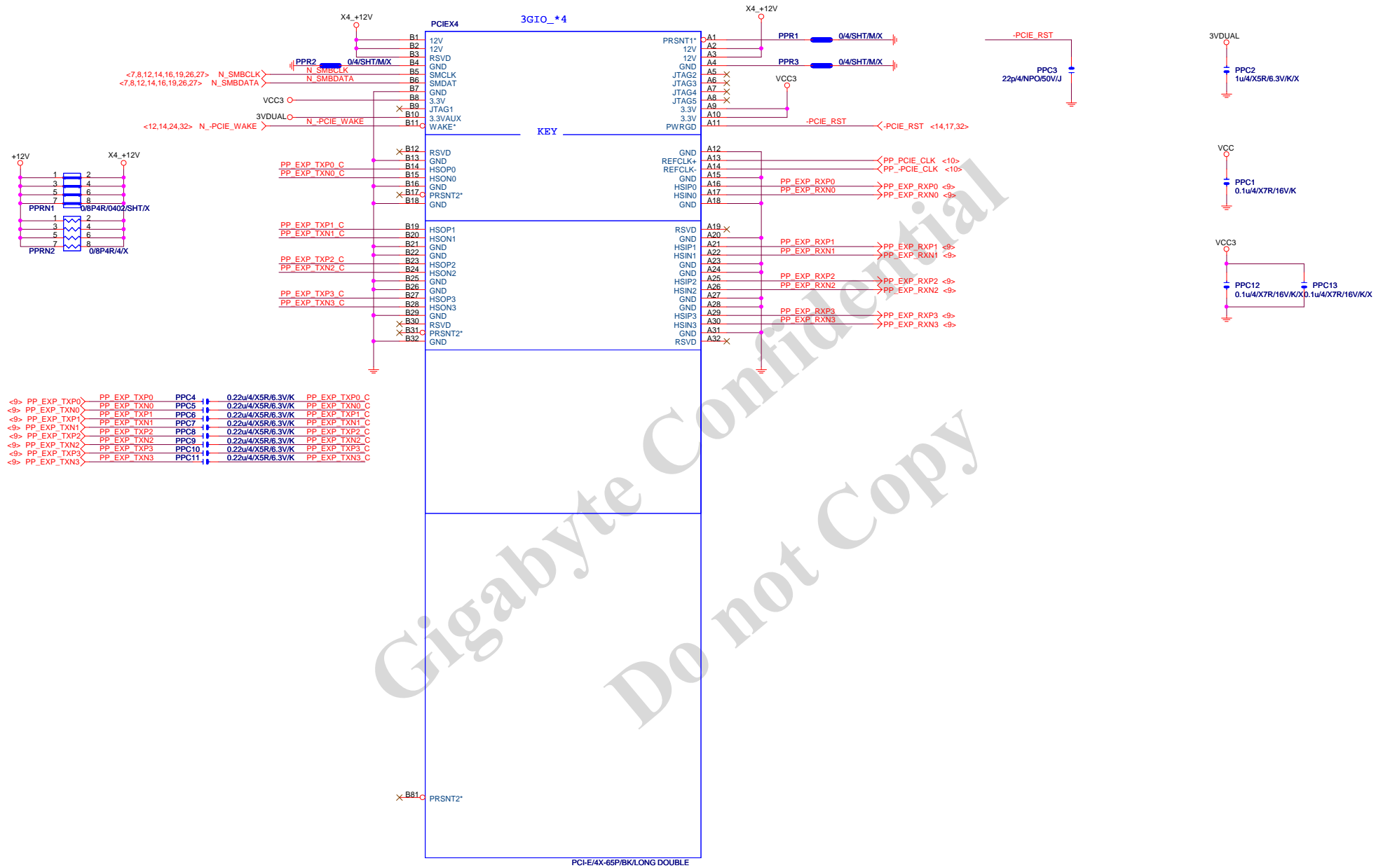


The auxillary reset circuit is only required for PCIe Gen3 margining and functional link training



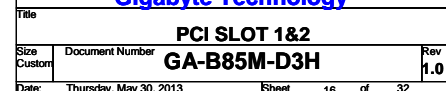
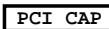
Gigabyte Technology		
Title PCI EXPRESS * 16		
Size Custom	Document Number GA-B85M-D3H	Rev 1.0
Date: Thursday, May 30, 2013	Sheet 14	of 32

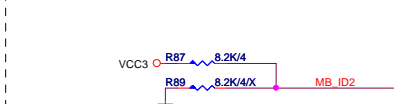
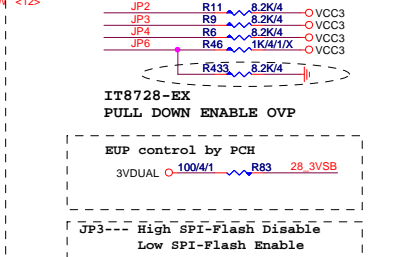
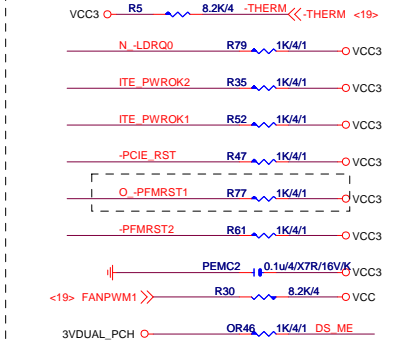
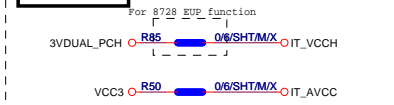
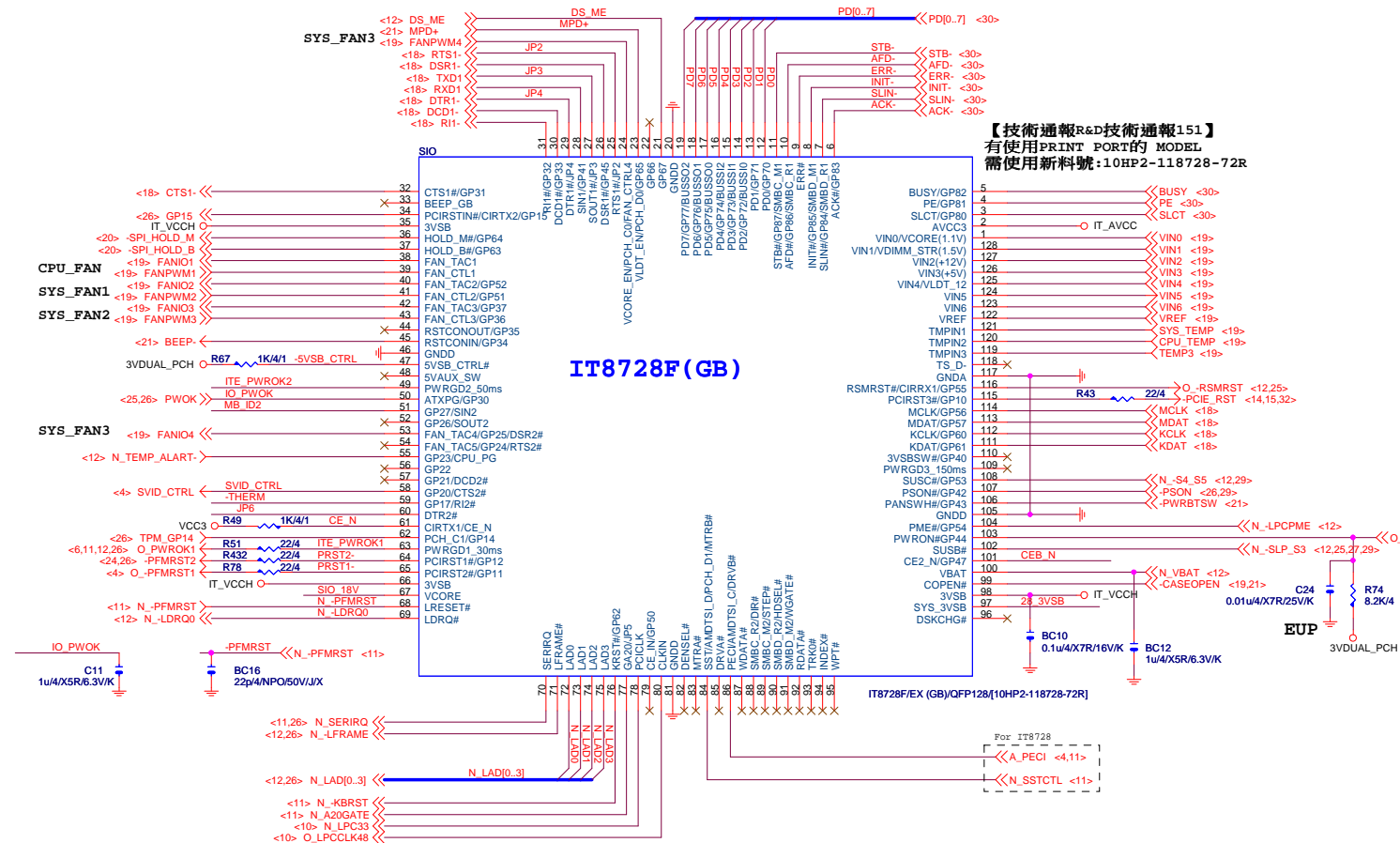
PCIEX4 SLOT



Gigabyte Technology

Title			PCI EXPRESS X 1 PORT
Size			Document Number
Custom			GA-B85M-D3H
Date:			Thursday, May 30, 2013
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Rev			1.0

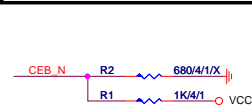




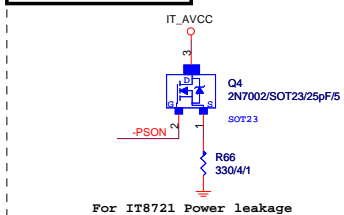
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDI_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSLI_D/MTRB# /PCH_D1
PIN55	PECI/AMDTSLI_C/DRVB#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

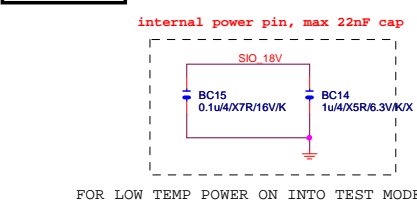
DUAL BIOS OPT STRAP



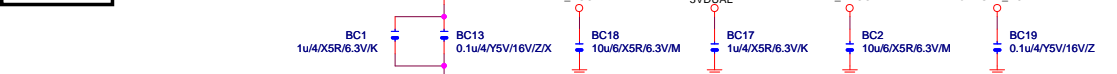
Power leakage



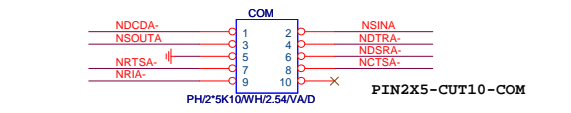
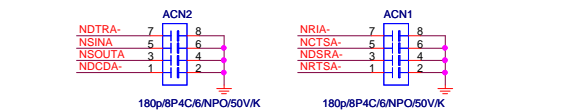
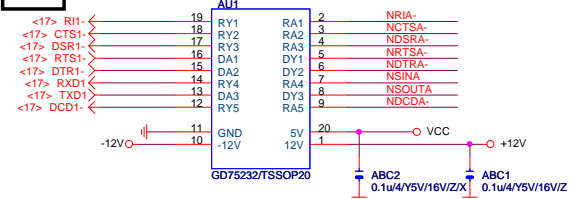
SIO_18V



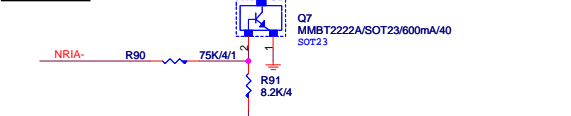
SIO CAP



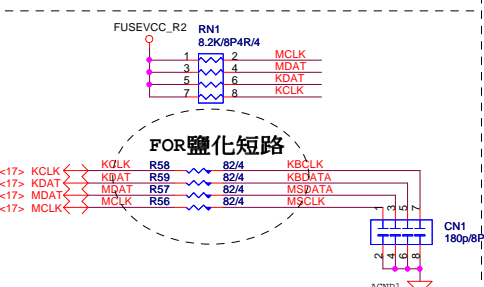
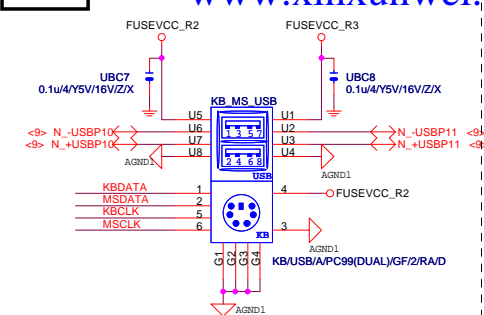
COM



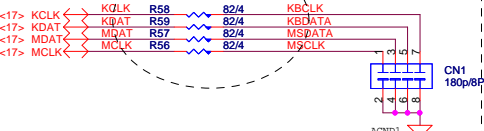
COM RI



KB/MS

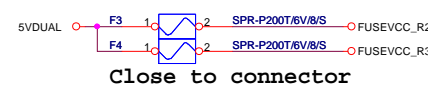


FOR鹽化短路



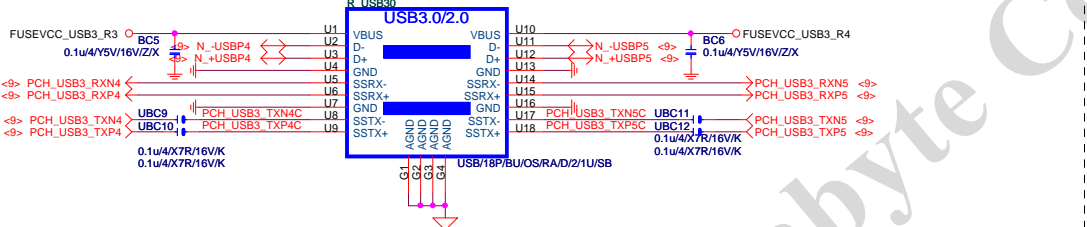
USB2.0 PWR

FUSE-0805

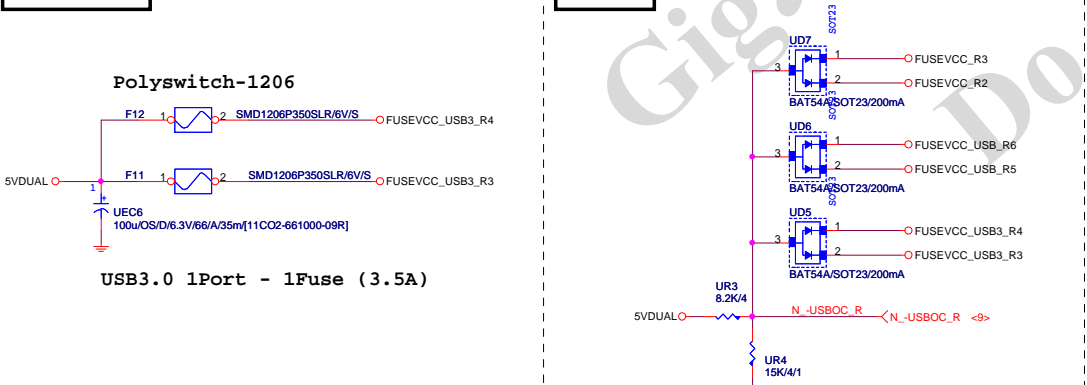


Close to connector

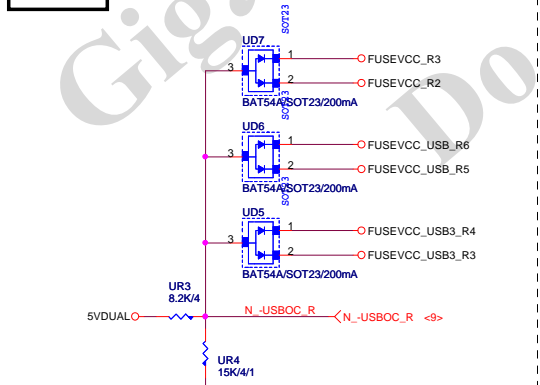
USB30_20



USB30_20 PWR

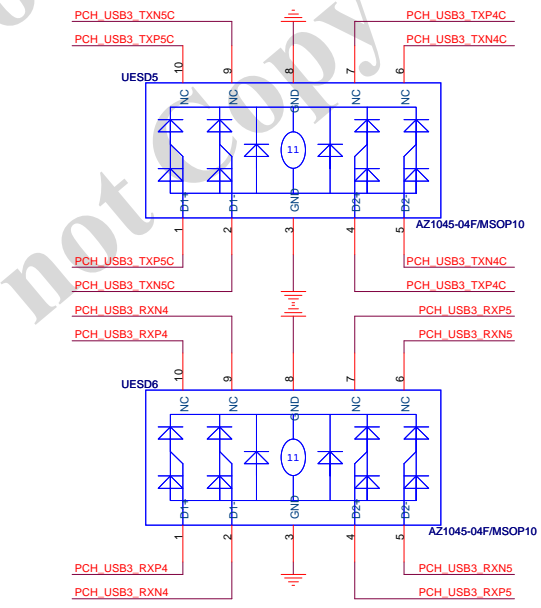


-USB0C_R

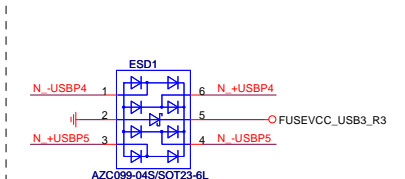


USB30_20 ESD PROTECT

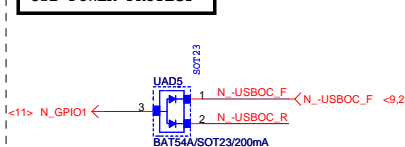
USB3.0 ESD



USB2.0 ESD



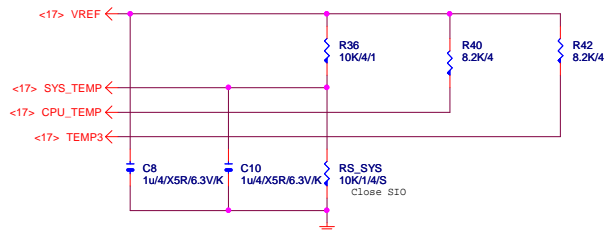
USB POWER PROTECT



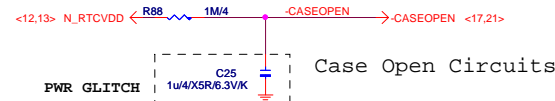
Gigabyte Technology

Title				COM-RI,KB_USB,USB_ESATA-PROCHOT	
Size				GA-B85M-D3H	
Date				Thursday, May 30, 2013	
Sheet				18 of 32	

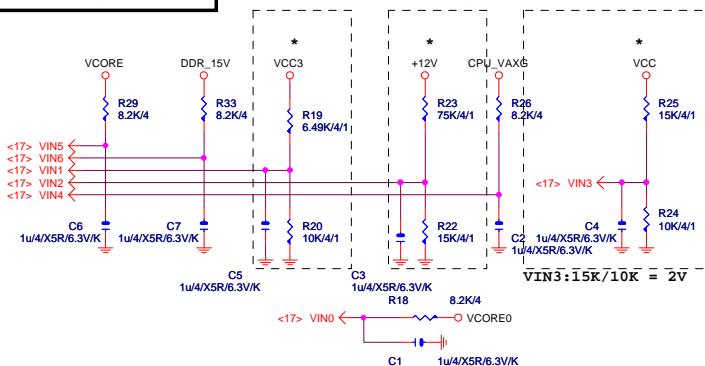
TEMP H/W MONITOR



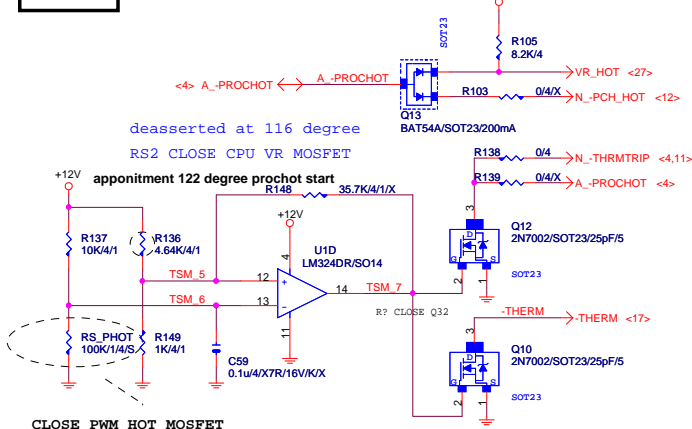
CASE OPEN



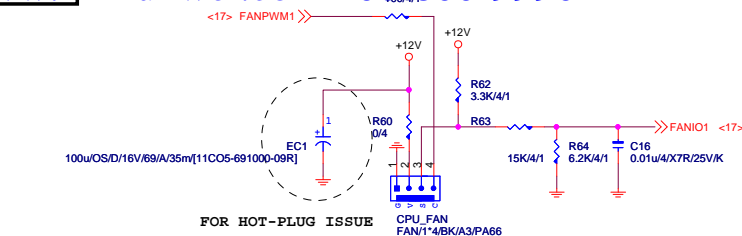
VOLTAGE-- H/W MONITOR



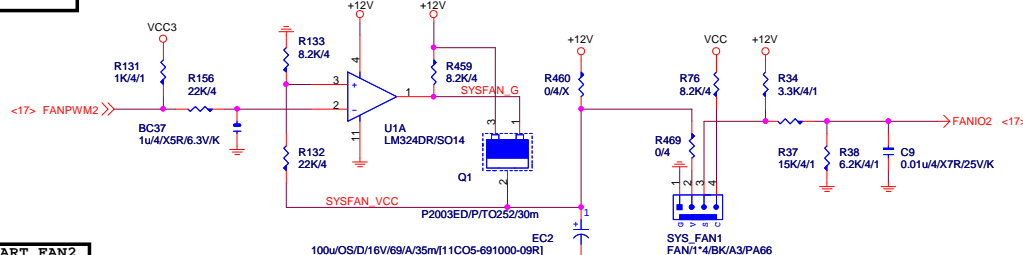
-PROHOT



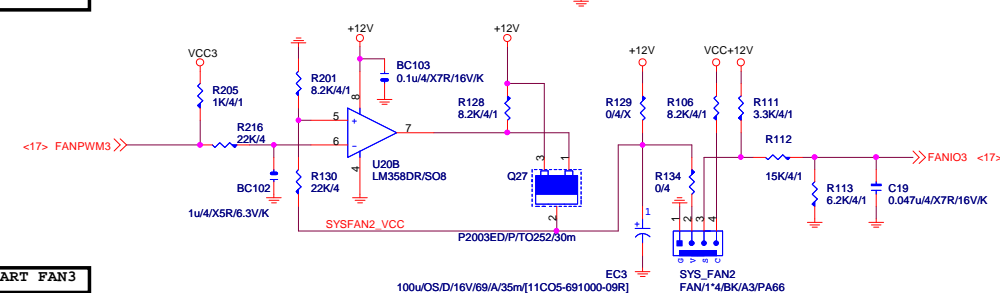
CPU SMART FAN



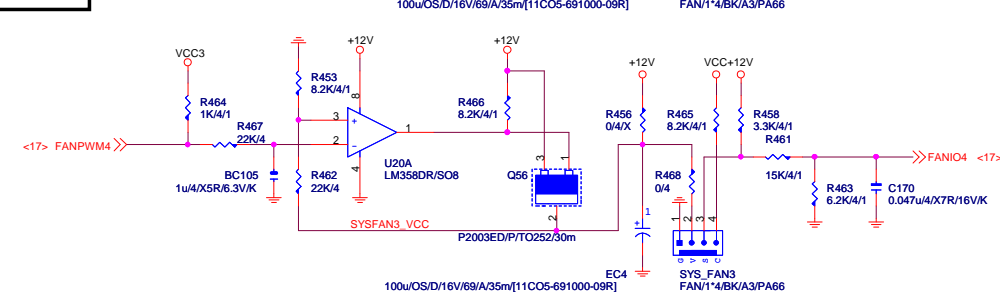
SYS SMART FAN



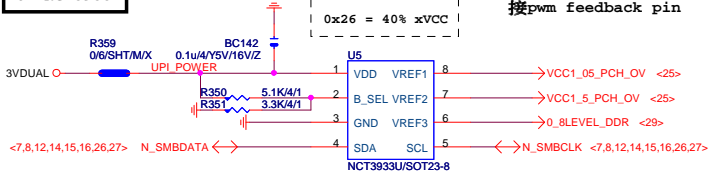
SYS SMART FAN2



SYS SMART FAN3

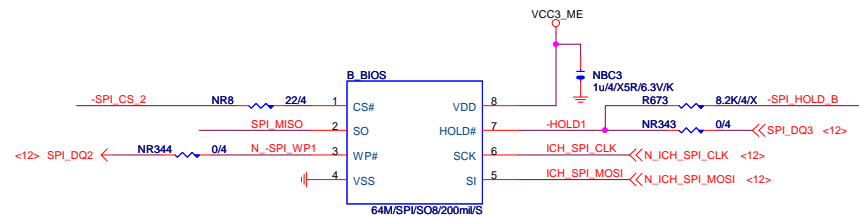
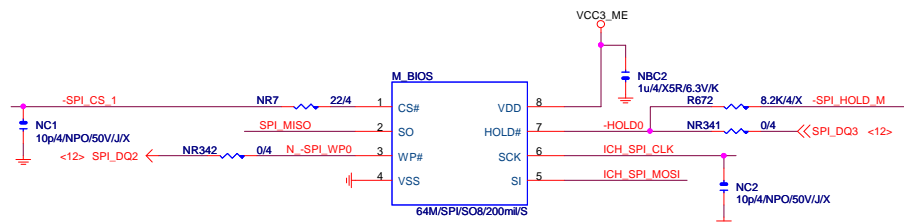


OV NCT3933



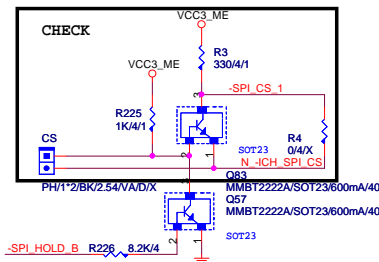
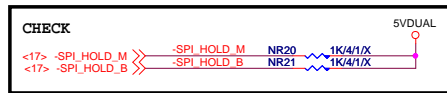
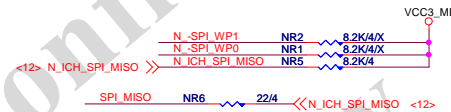
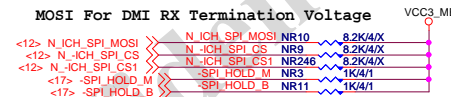
Gigabyte Technology

Title	HWM,FAN CTRL,OV		
Size	Document Number	GA-B85M-D3H	
Custom	Rev	1.0	
Date:	Thursday, May 30, 2013	Sheet	19 of 32

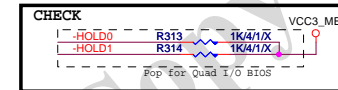
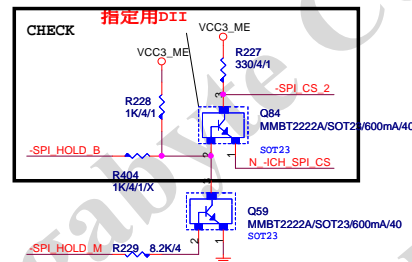


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

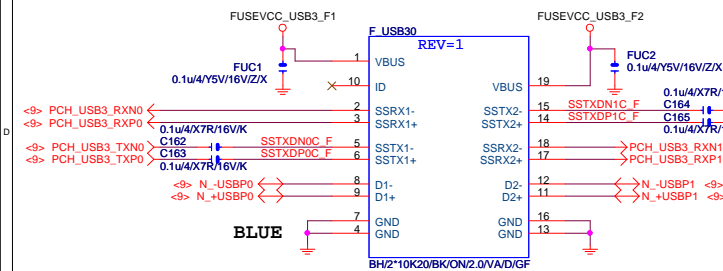
1 means floating
0 means PD 1k



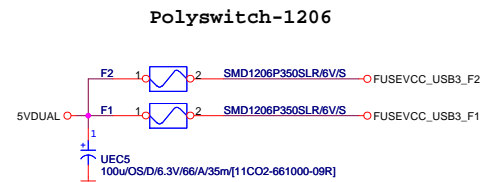
Dual BIOS CS connect
circuit update



F_USB30

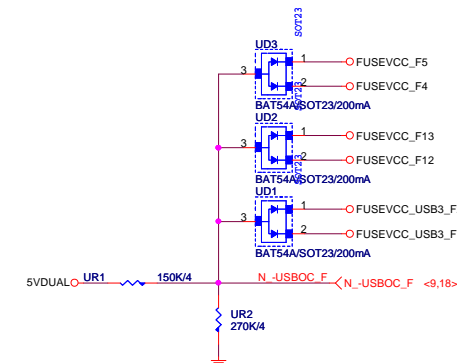


F_USB30 PWR

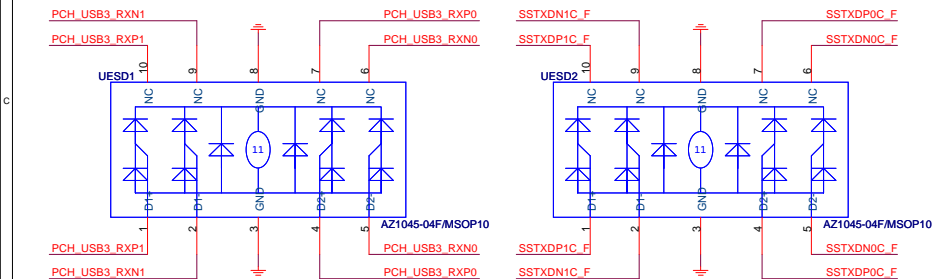


USB3.0 1Port - 1Fuse (3.5A)

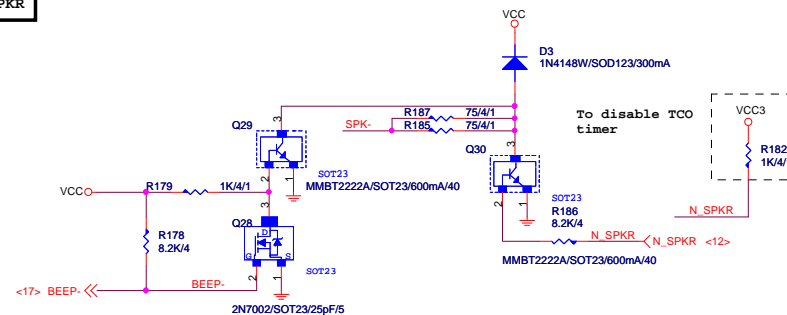
-USBOC_F



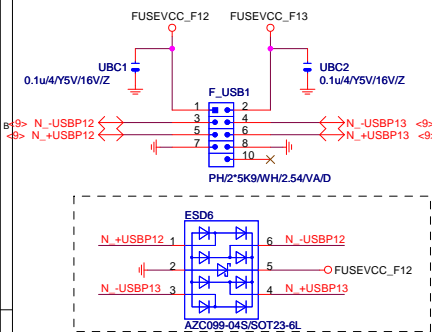
F_USB30 ESD PROTECT



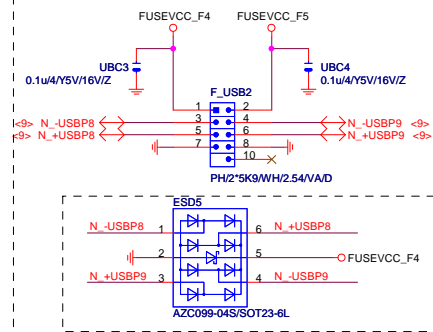
SPKR



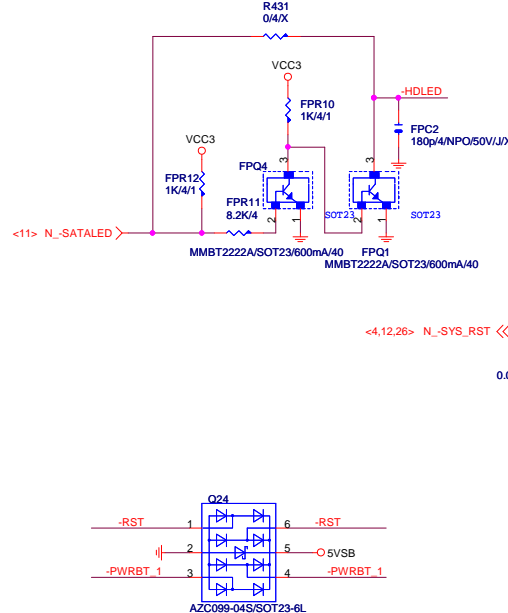
FRONT USB1



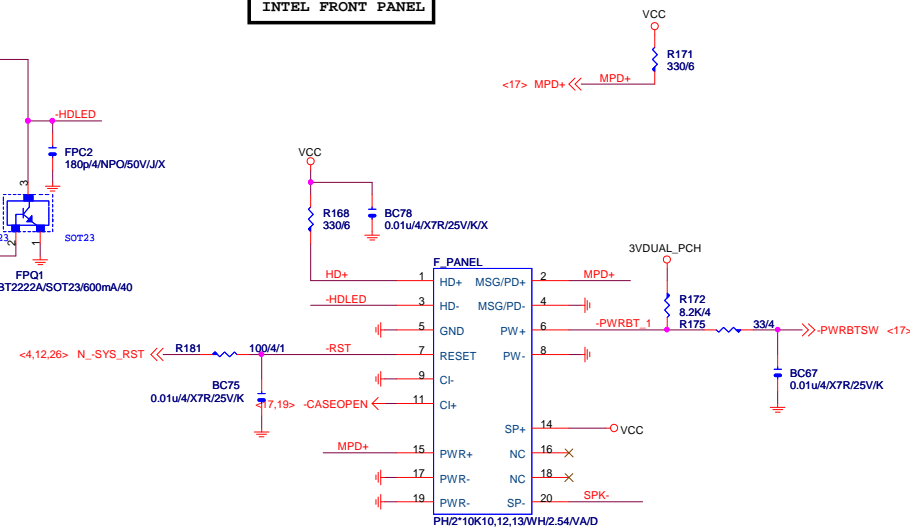
FRONT USB2



SATA LED



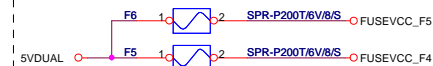
INTEL FRONT PANEL



FUSE-0805



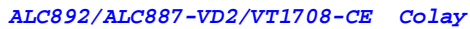
FUSE-0805

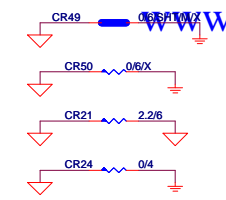


Gigabyte Technology

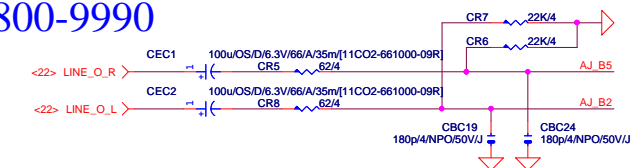
Title			
FP,F_USB,USB PWR,SPKR,SATA LED			
Size	Document Number	Rev	
Custom	GA-B85M-D3H	1.0	
Date:	Thursday, May 30, 2013	Sheet	21 of 32

ALC892/ALC887-VD2/VT1708-CE Colay



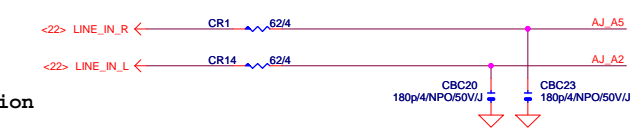


LINE-OUT



Only reserved for ALC888

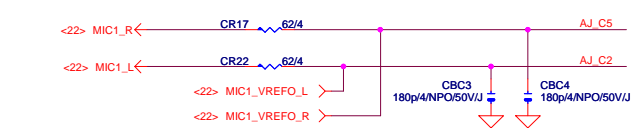
LINE-IN



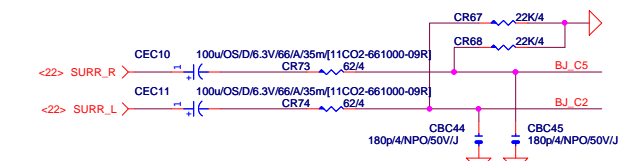
Verify MIC function in LINE-in

For 889A/888

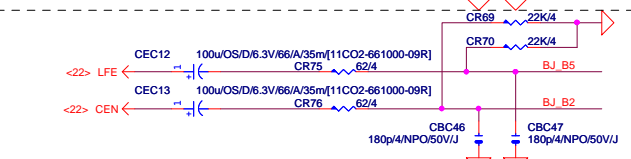
MIC-IN



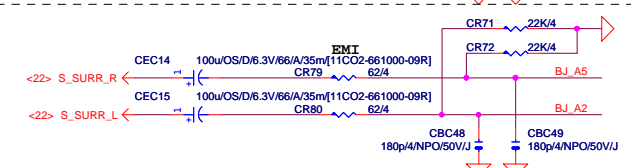
SURROUND



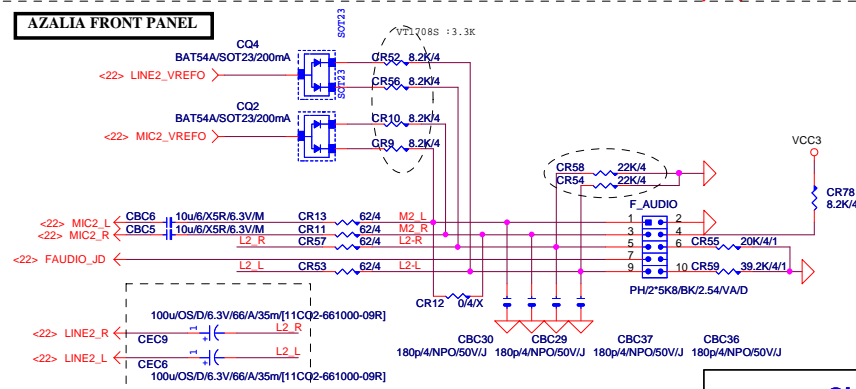
CEN/LFE



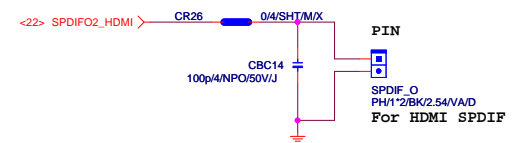
SURR BACK



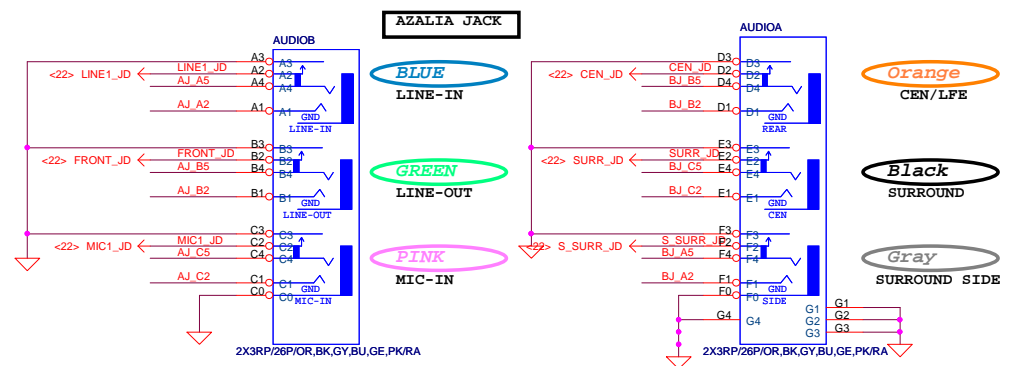
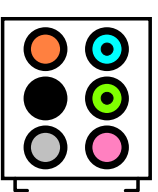
AZALIA FRONT PANEL

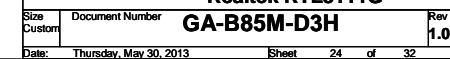
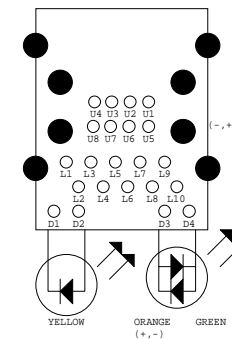


SPDIF_OUT



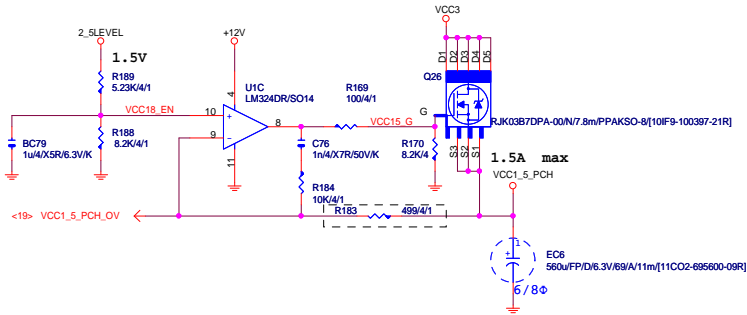
AZALIA JACK



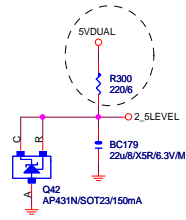


注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]

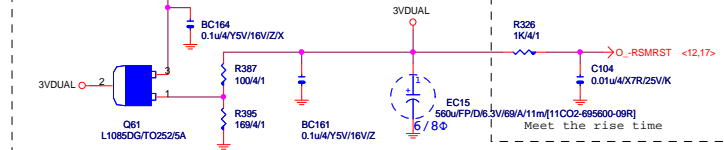
VCC1_8_PCH



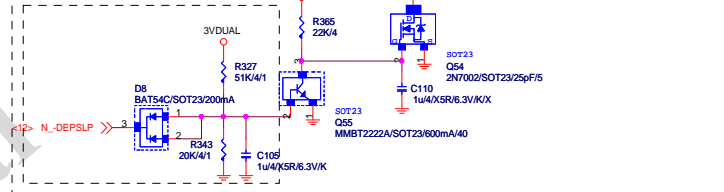
ERP



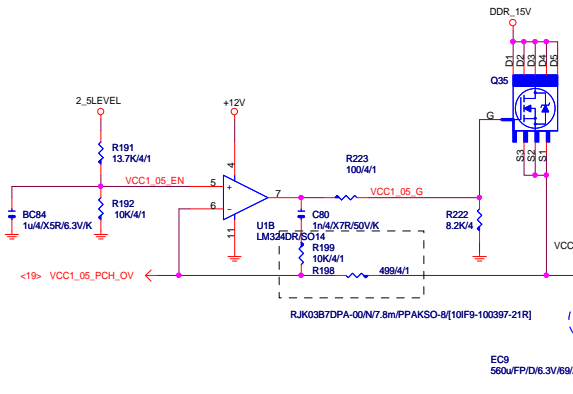
3VDUAL



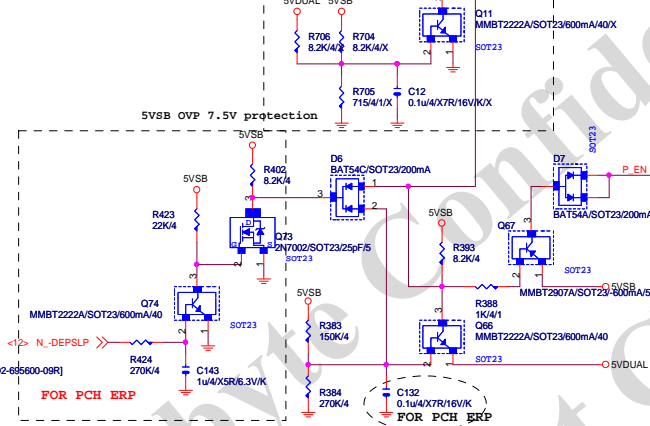
-RSMRST



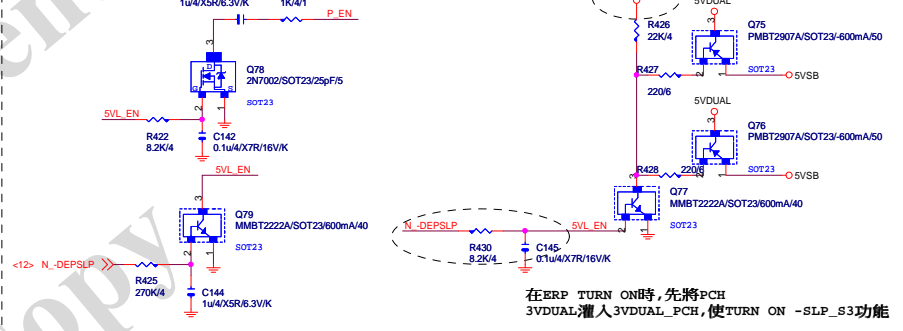
VCC1_05_PCH



5VDUAL SHORT PROTECT

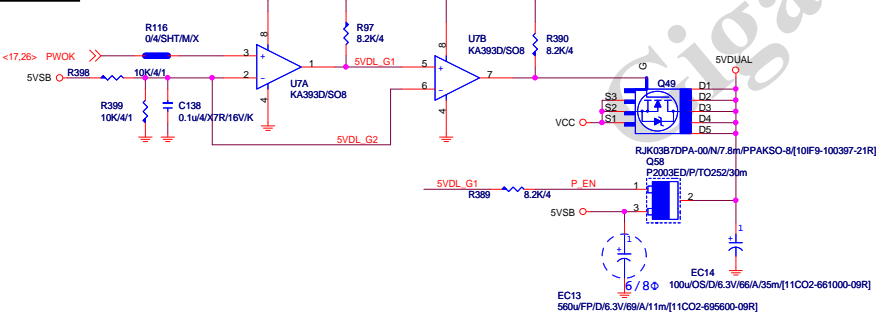


PCH ERP

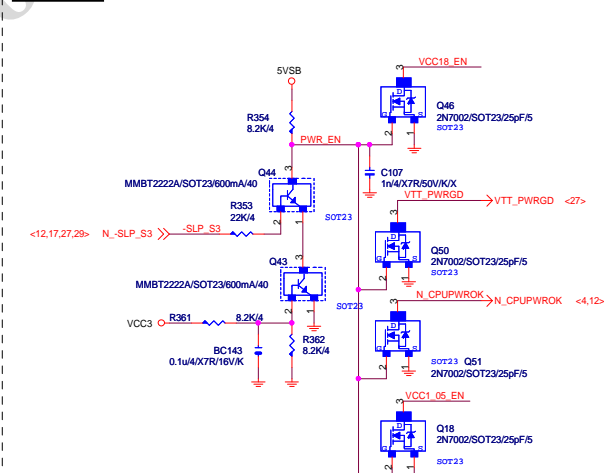


在ERP TURN ON時, 先將PCH 3VDUAL灌入3VDUAL_PCH, 使TURN ON -SLP_S3功能

5VDUAL



PWR SEQ



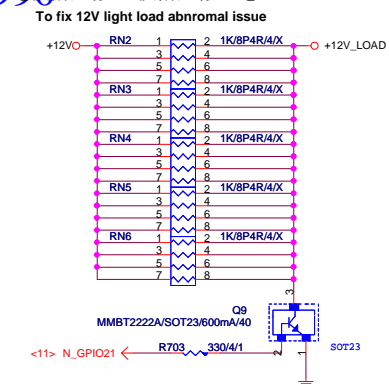
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DISCRETE POWER

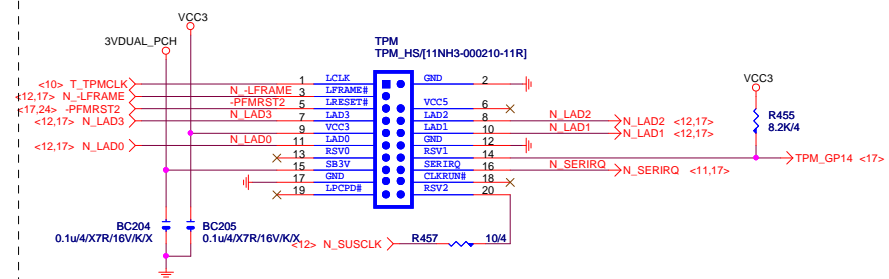
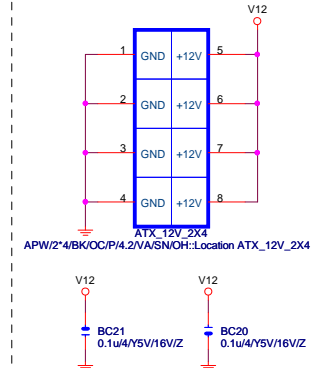
GA-B85M-D3H

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ATXX4 POWER CONNECTOR

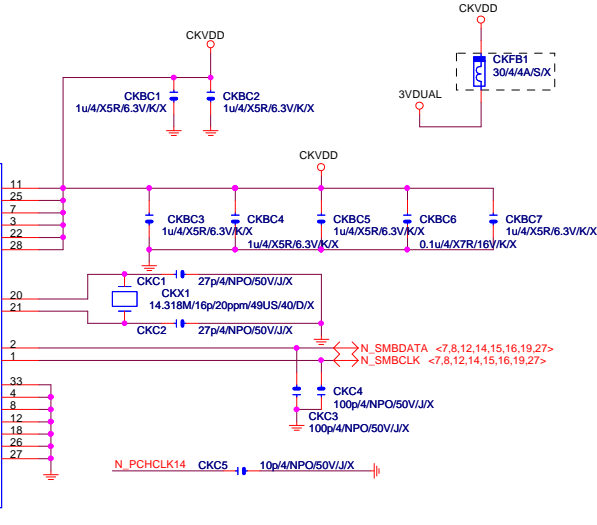


CPU Frequency Selection

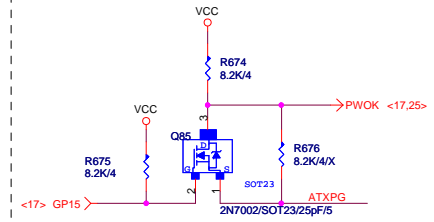
The diagram illustrates the pinmux configuration for the 9LRS41058B17/MLF32X2. It shows the mapping of internal signals to physical pins and their functions. Key components include:

- CKVDD:** Power supply pins for the clock core, connected to CKR8, CKR1, CKR2, and CKR3.
- CLK:** Clock signal pins, including DOC_0, DOC_1, CPUT_LR, CPUC_LR, SATALCKT_LR, SATALCKC_LR, PCIEXT_LR, PCIEXC_LR, DOT96T_LR, and DOT96C_LR.
- SDATA:** Serial data pins, including SCL.
- GPIO:** General-purpose input/output pins, including GNDPAD, GNDPCPU, GNDPCIE, GND96, GNDREF, GNDSDA, and GND25.
- Other pins:** VDD96, VDDPCIE, VDDCPU, VDDREF, VDD25, LPC_48, CPU_STP, CBKBC8, and VCC3.

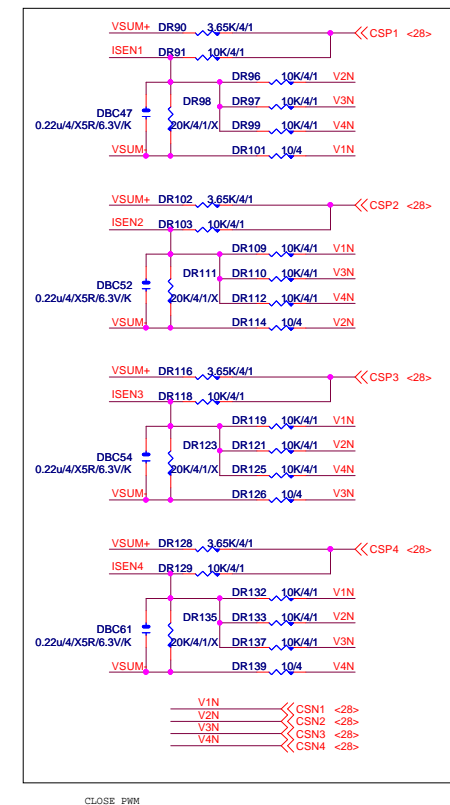
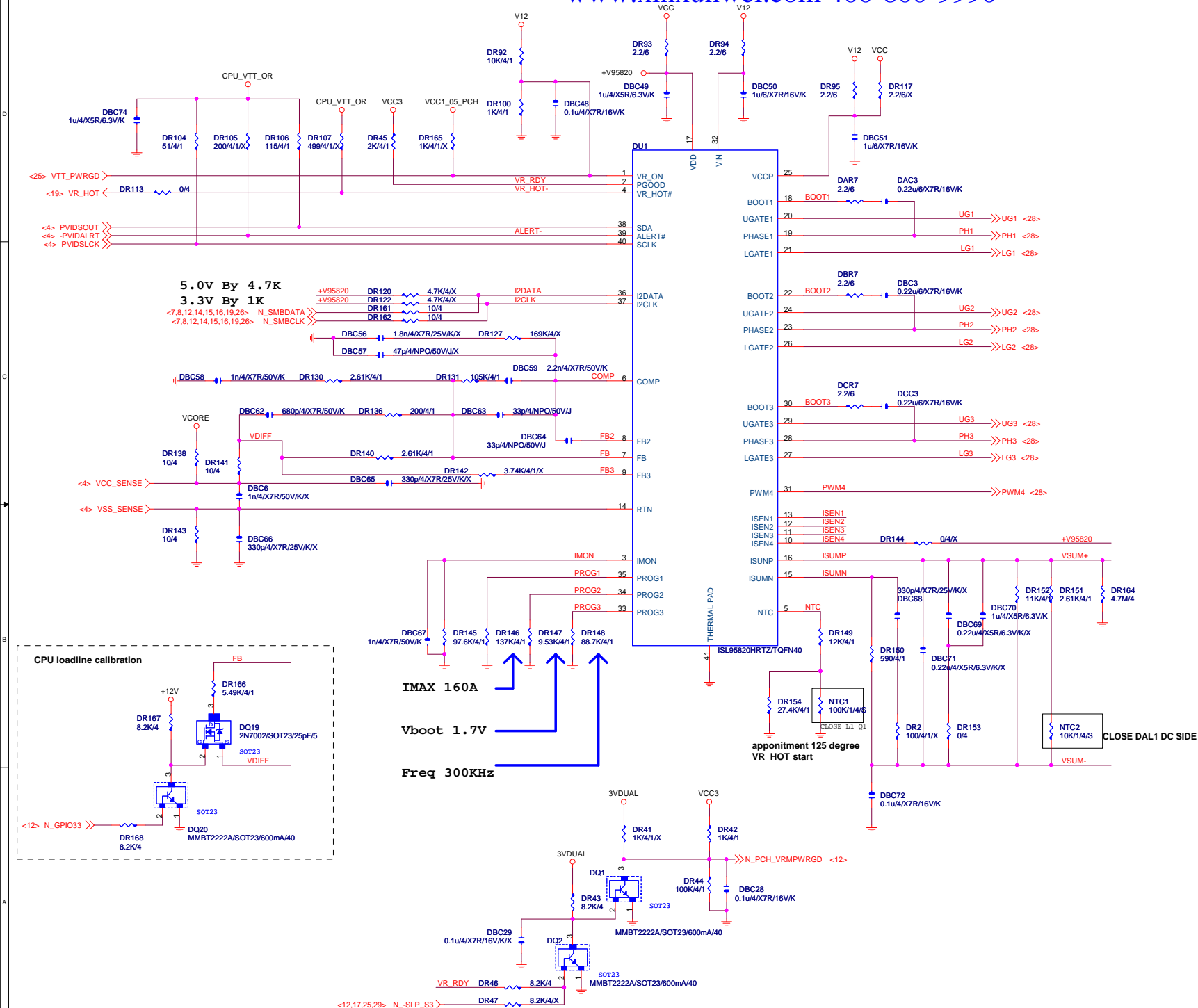
The diagram also shows the connection of various peripheral modules, such as the CPU, CPUC, SATALCK, PCI, and SDATA, to the pinmux. The pinmux is configured to support the 9LRS41058B17/MLF32X2 device.

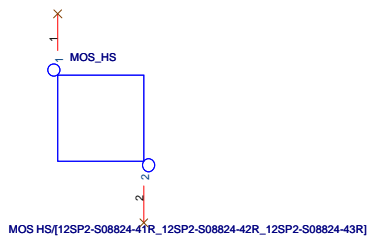
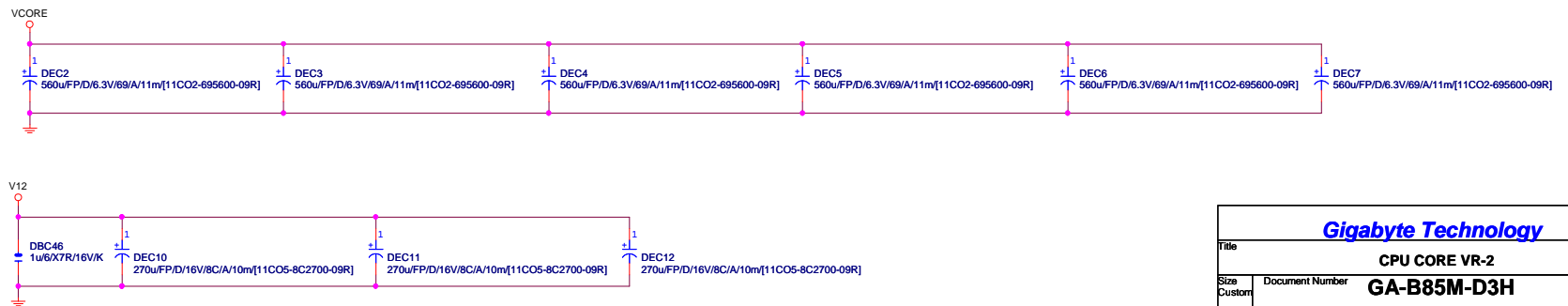
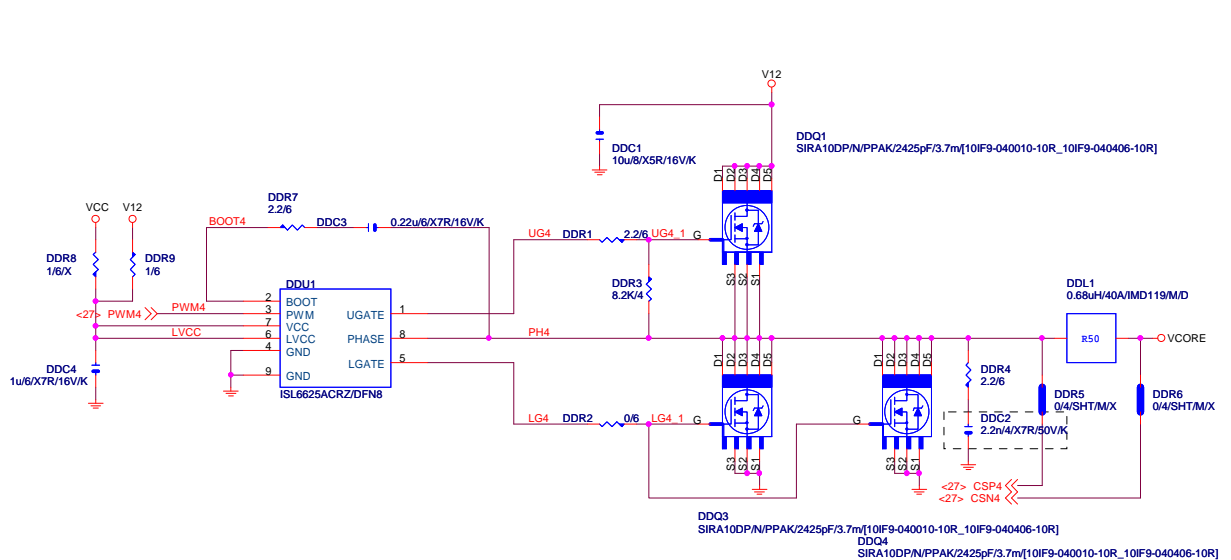
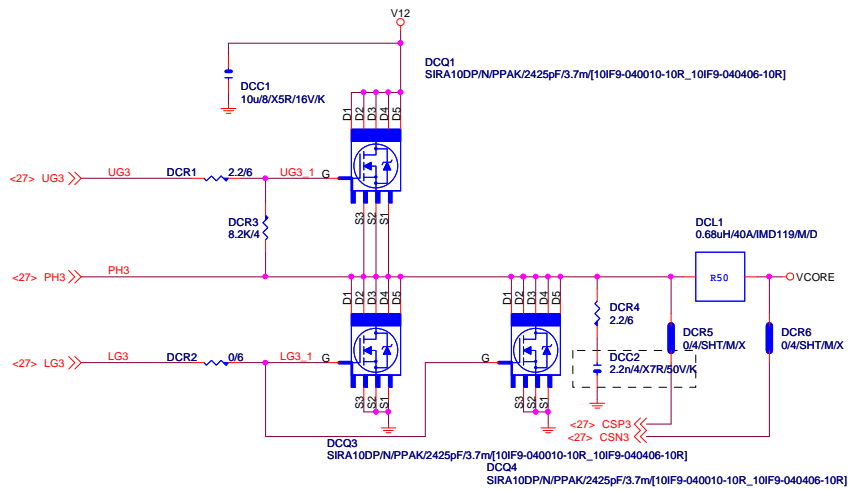
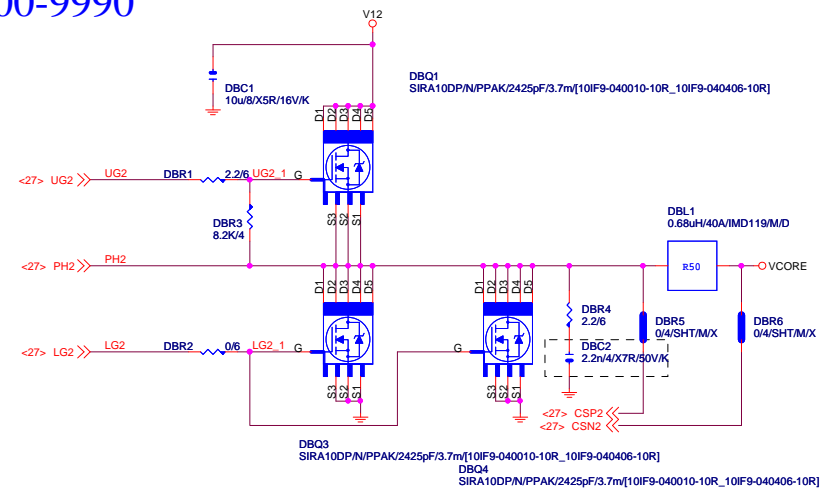
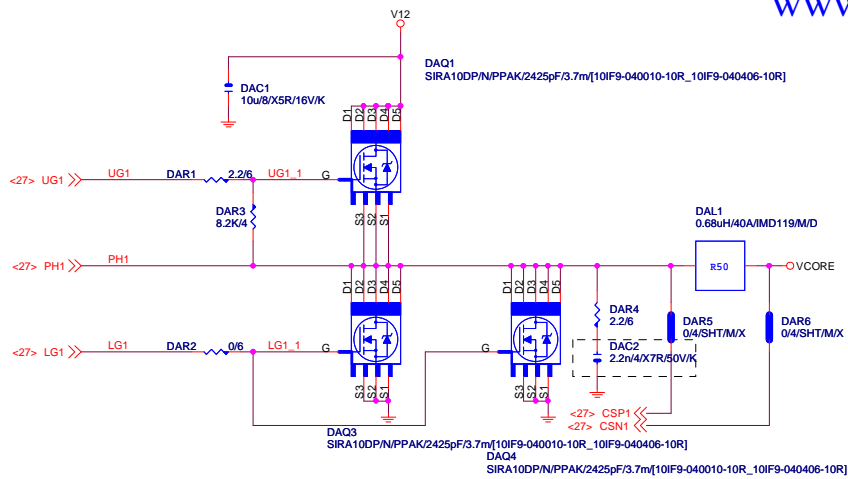


【技術通報R&D技術通報154】

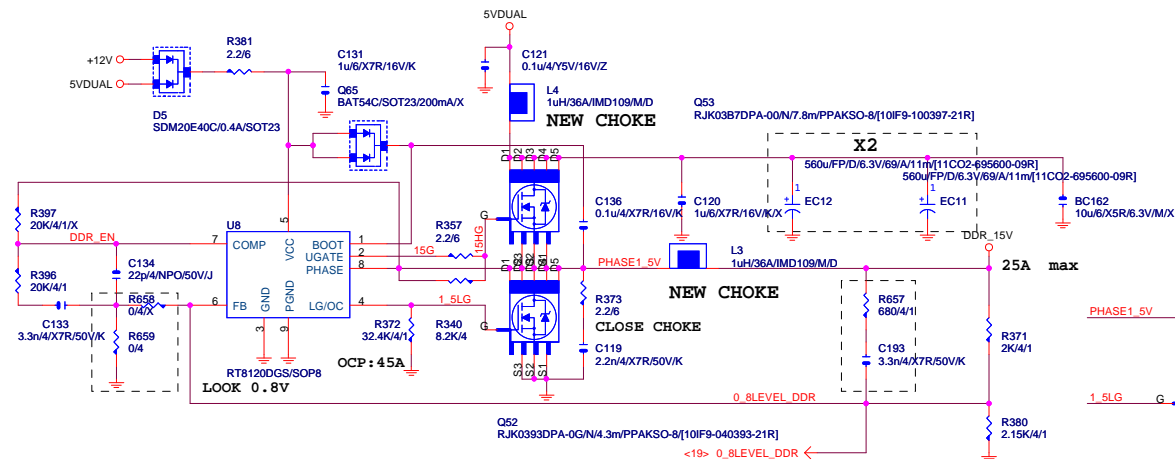


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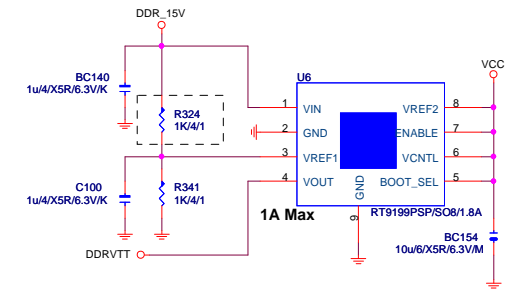




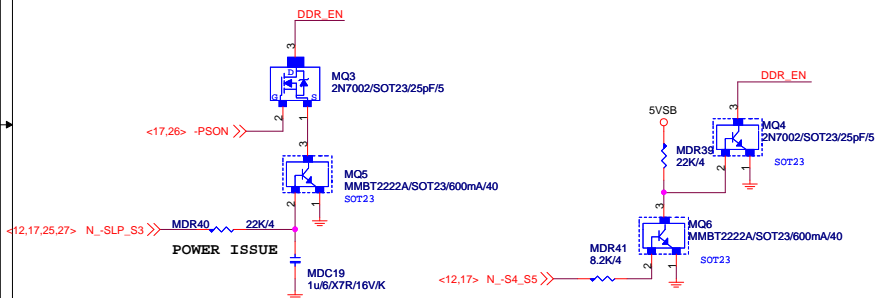
DDR15V



DDRVRTT



PWR SEQ



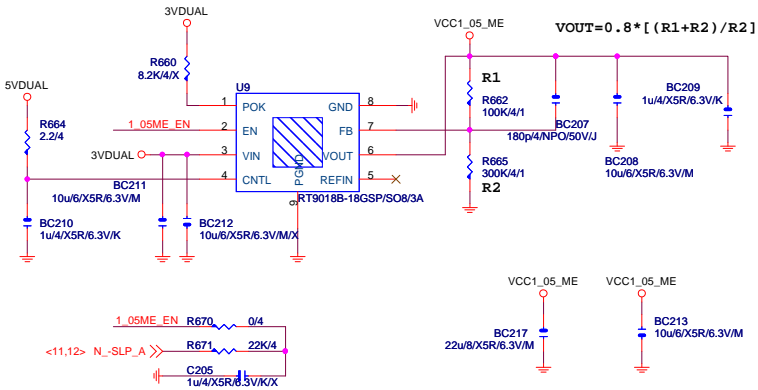
VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
 IRMS=11.45A
 560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
 Coefficient=1.7(85°C), 1(105°C)
 VIN Ripple current=4.7X1.7=7.99A(85°C)
 -->故固态电容须2X7.99=15.98>11.45A

$R_{ocset} = (I_{ocp} * L_{gate}, rdson) / I_{ocset}$
 $R_{ocset} = (45A * 6.7m\Omega) / 10\mu A = 30K$
 $I_{ocset} = 10\mu A$

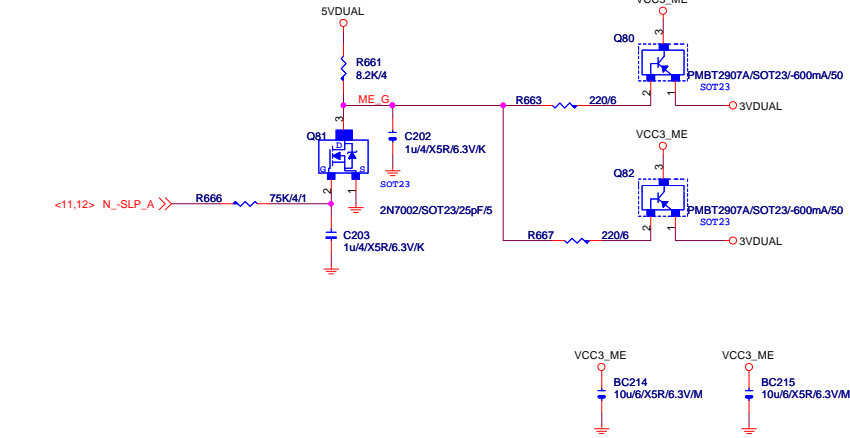
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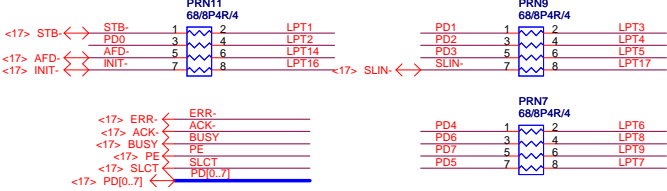
VCC1_05_ME



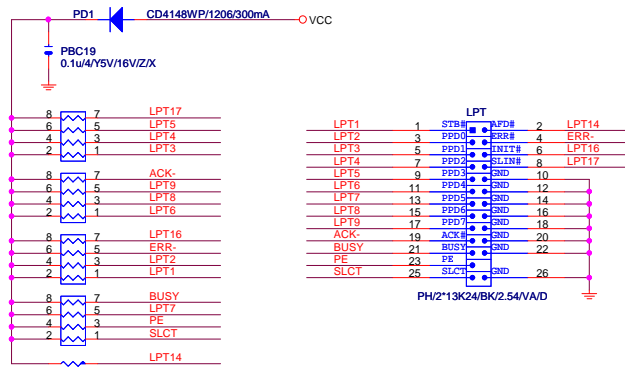
VCC3_ME



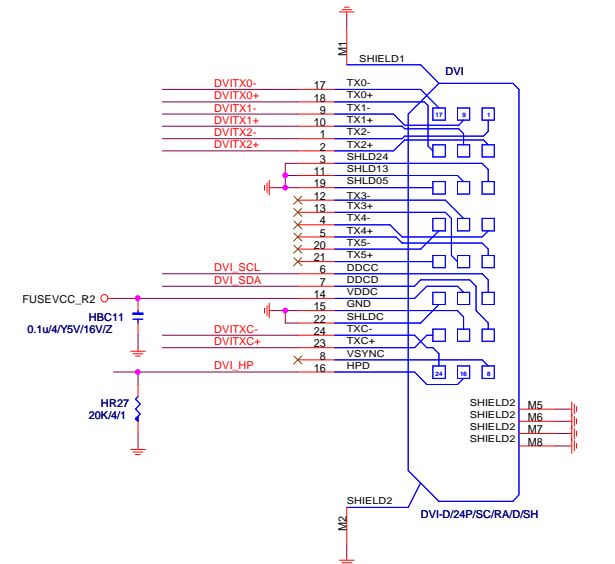
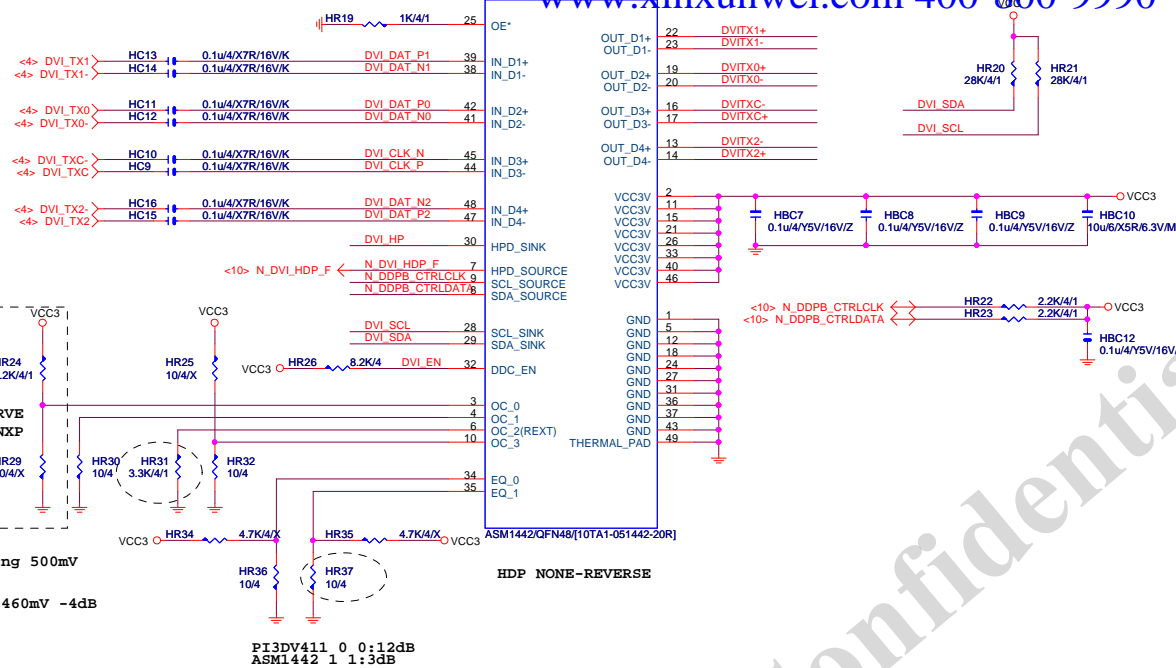
LPT PORT



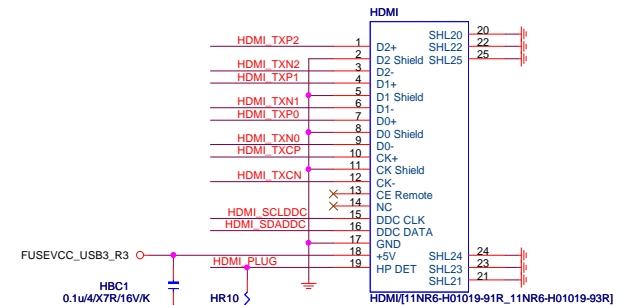
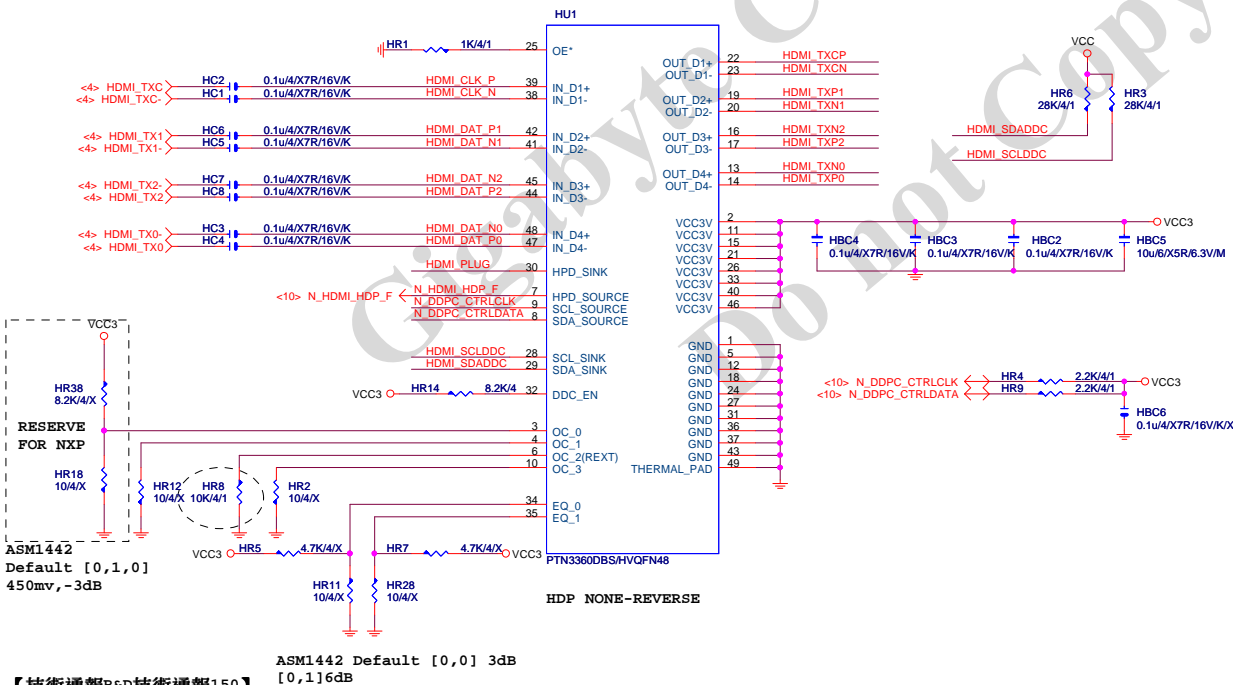
【技術通報R&D技術通報151】
33ohm Change to 68ohm



DVI LEVEL SHIFT



HDMI LEVEL SHIFT



【技術通報R&D技術通報150】

HDMI eye diagram 1.4版(deep color)會fail

原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

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